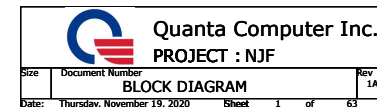
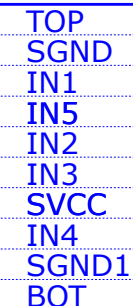

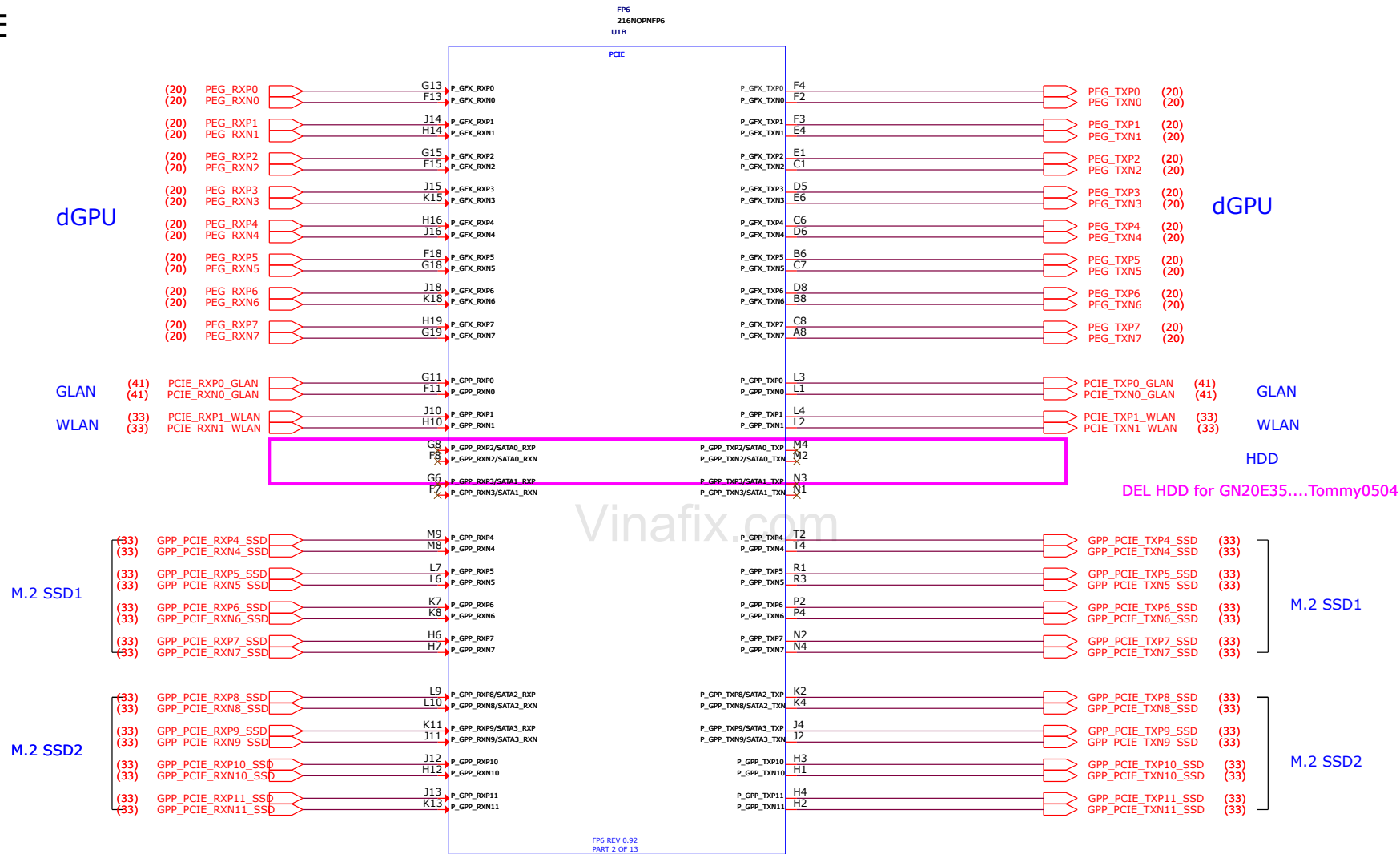


## 01



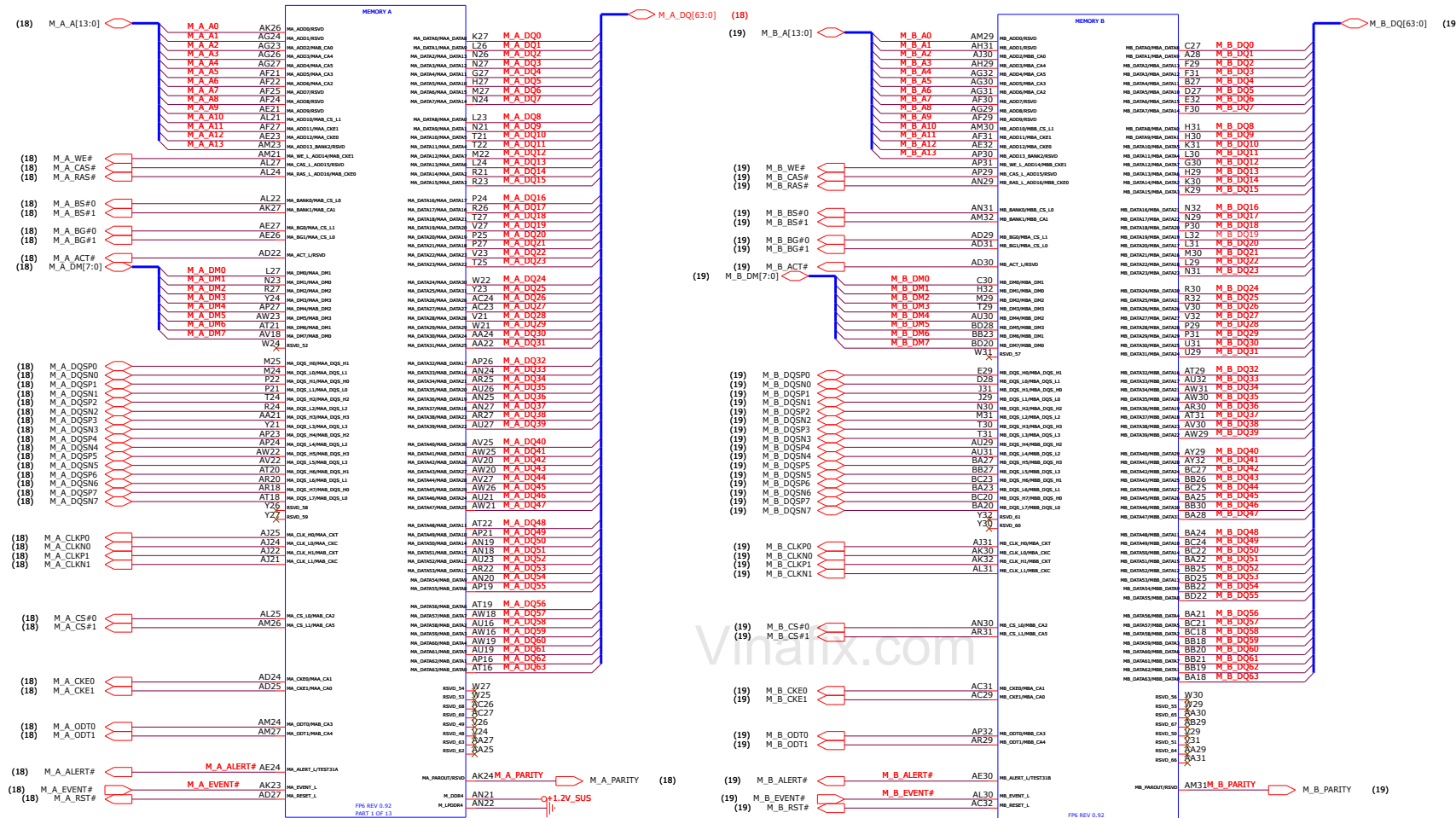
02

Model	REV	CHANGE LIST									
FA506/706 (QM/QR)	SR to ER	Item	Stage	Page	Owner	Change explanation					
		01	ER	33	EE	ER01	: Support PLDR add BT_Disable# and WLAN_Disable#				
		02	ER	30	EE	ER02	: Change USB2.0 ESD SD19 .SD20. SD21 Diode for ASUS request.				
		03	ER	31	EE	ER02	: Change USB2.0 ESD SD19 .SD20. SD21 Diode for ASUS request.				
		04	ER	06	EE	ER03	: Add R886 for EC initial (SPICK_EN) .				
		05	ER	06	EE	ER04	: Change GPIO pin AGPIO91 to AGPIO21 for Modern Standby request.				
		06	ER	08	EE	ER05	: Reserved for APU power sequence (+0.75V_S5 --> +1.8V_S5 --> +3V_S5)				
		07	ER	36	EE	ER06	: Reserved SPDIF-OUT pull-down 10kohm				
		08	ER	39	EE	ER07	: Change FAN connector from 5-pin to 4-pin for CN13 and CN14 .				
		09	ER	29	EE	ER08	: Reserved SD22 for ESD request .				
	ER to PR	01	PR	05	EE	PR01	: R4,R6,R22 Change 1K from 100K for LCD panel PSR issue.				
		02	PR	06	EE	PR02	: Add R890 and short pad R94 for SPI_CLK waceform.				
		03	PR	17	EE	PR03	: Add S13 GASKET for EMI request.				
		04	PR	22	EE	PR04	: Reserved VC5729 ,VC5730 for Power malfunction, GPU lost.				
		05	PR	22	EE	PR05	: ROM_SCLK follow NVDIA CRB board pull-up.				
		06	PR	23	EE	PR06	: Remove VR5087 , follow NVDIA CRB baord.				
		07	PR	29	EE	PR07	: Change F1 from 1.5A to 2.5A for Factory issue.				
		08	PR	30	EE	PR08	: Change CC1 & CC2 ESD to single pin for SD19 leakage issue on Type C port.				
		09	PR	30	EE	PR09	: Change SU13 VIN (pin3) from +1.8V_S5 to +3V_S5 for power plane is not enough.				
		10	PR	33	EE	PR10	: Un-mount R853 for power management by customer's table list.				
		11	PR	33	EE	PR11	: Un-mount R887 , R888 (WLAN & BT do not support PLDR)				
		12	PR	35	EE	PR12	: Change TU1 power rail from 51225_LDO3 to +3V for power consumption under 0.4mA on bettery mode .				
		13	PR	35	EE	PR13	: Change TU2 power rail from 51225_LDO3 to +3V for power consumption under 0.4mA on bettery mode .				
		14	PR	37	EE	PR14	: Change KU1 LPC LAD0~LAD3 topology for ESD issue.				
		15	PR	37	EE	PR15	: Reserved KR128 for S0i3 , EC GPC3 used for dGPU ID for E5 & E3				
		16	PR	37	EE	PR16	: Reserved KR118 for LID_SW CMOS type ; Reserved KR121 for bettery mode power consumption.				
		17	PR	38	EE	PR17	: Un-mount KPSW1 , debug only for SR & ER stage .				
		18	PR	38	EE	PR18	: Change KHE1 power rail from +3VPCU to +3V_S5 for power consumption under 0.4mA on bettery mode .				
		19	PR	41	EE	PR19	: Reserved R855 for power management by customer's table list.				
		20	PR	37	EE	PR20	: Mount KESD3 , KESD4 for ESD issue.				
	PR to MP	01	MP	06	EE	MP01	: Mount R83 for PCIe_WAKE#				
		02	MP	35	EE	MP02	: Change TU1 and TU2 power rail from +3V to 51225_LDO3				
		03	MP	38	EE	MP03	: Add KHE1 power rail from +3V_S5 to +3V_PCU.				
		DOC NO.		PROJECT MODEL :	NJF	APPROVED BY:		DATE:	2019/06/15		
				PART NUMBER:		DRAWING BY:		REVISION:	1A		
										<div><div></div><div>Quanta Computer Inc. PROJECT : NJF Change list</div></div>	

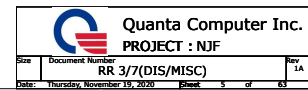


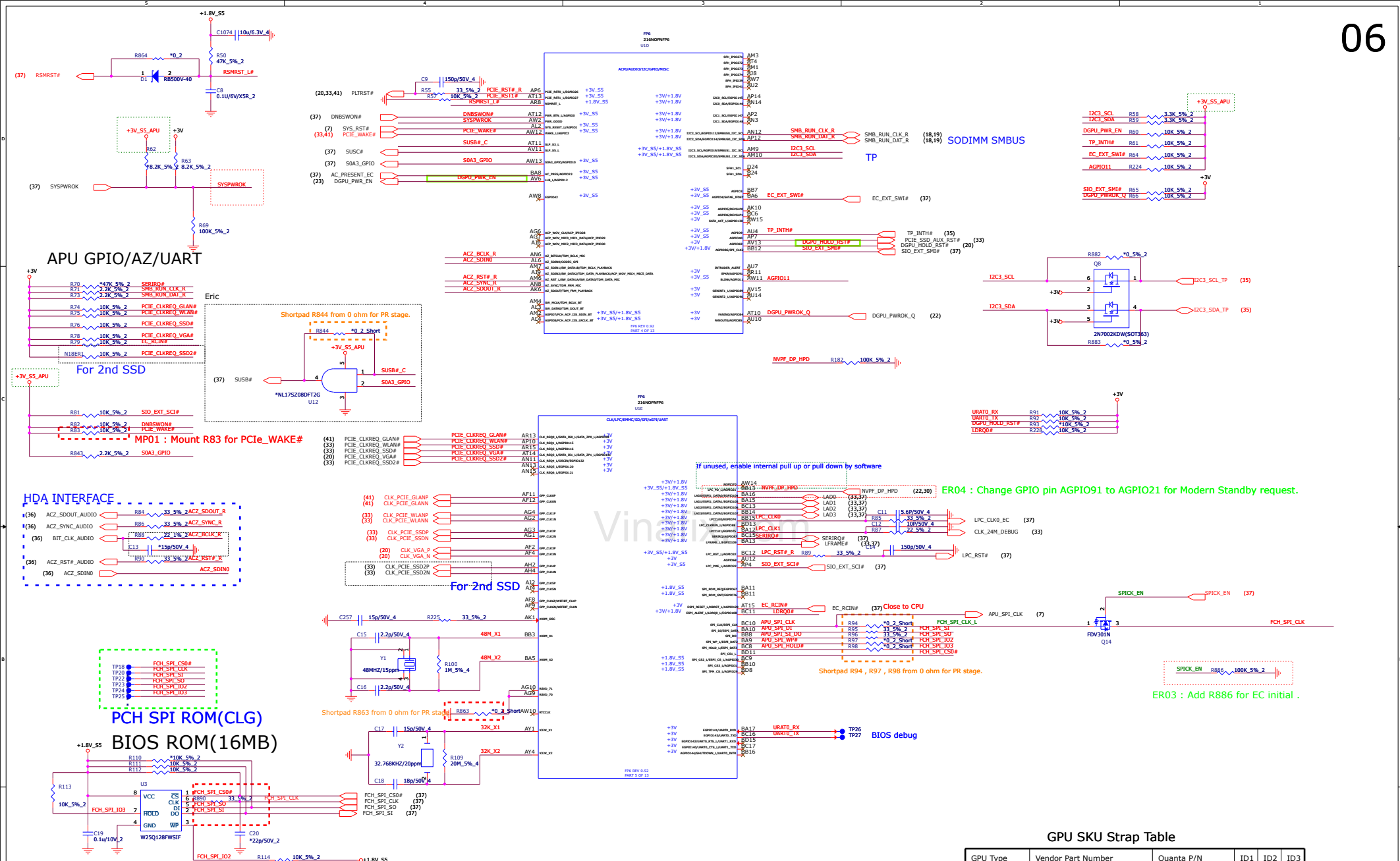
Quanta Computer Inc.  
PROJECT : NJF

# APU MEMORY



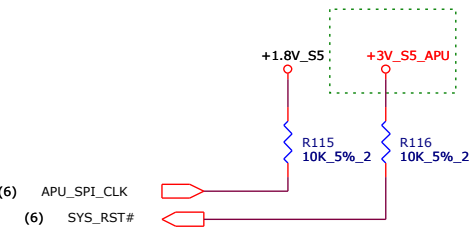
04





USB2 Port	Function
USB0	TYPE-C
USB1	U3B PORT1
USB2	
USB3	Camera
USB4	U3B PORT3
USB5	U3B PORT2
USB6	Bluetooth
USB7	

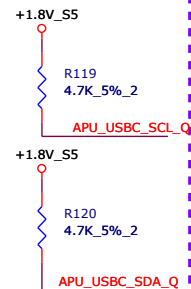
## STRAPS PINS



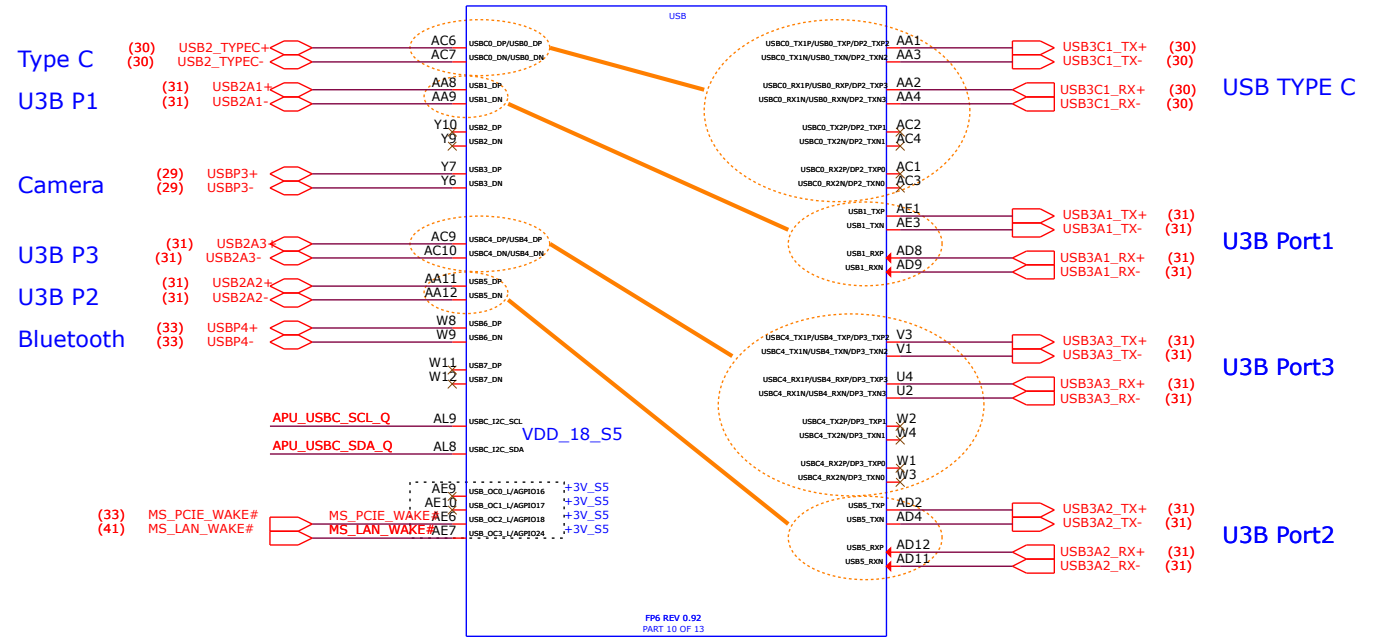
## REQUIRED STRAPS

	APU_SPI_CLK	SYS_RST# <i>Int Pull-Up</i>
PULL HIGH	Use 48Mhz crystal clock and generate both internal and external clocks <b>DEFAULT</b>	normal reset mode <b>DEFAULT</b>
PULL LOW	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

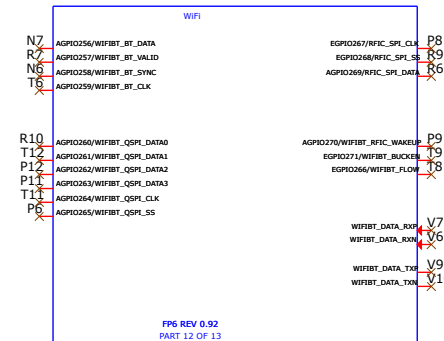
## 180110 ADD for re-driver



## USB3 and USB2 Port Mapping

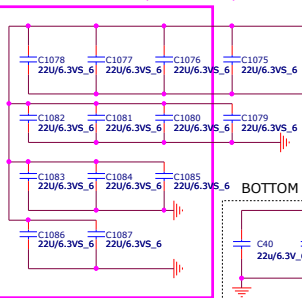


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FP6  
216NOPNFP6  
U11

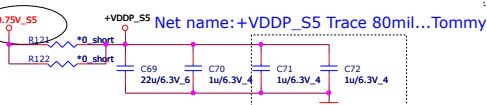
Quanta Computer Inc.  
PROJECT : NJF

Add 22 x13 for CZ request!...Tommy

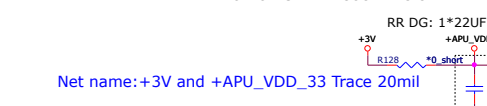


Net name: +0.75V\_S5 Trace 80mil from PL70 to R1244,R1221...Tommy

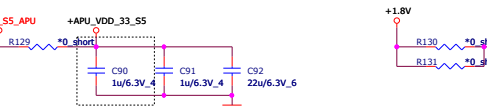
RR DG: 1\*22UF+3\*1UF



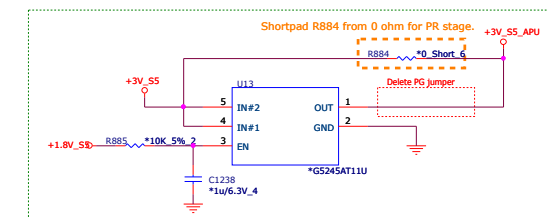
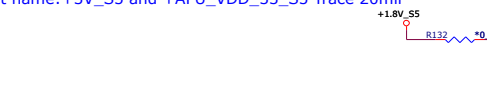
RR DG: 1\*22UF+2\*1UF



RR DG: 1\*22UF+2\*1UF

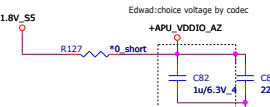


Net name: +3V\_S5 and +APU\_VDD\_33\_S5 Trace 20mil



RR DG: 1\*22UF+1\*1UF

Max: 0.2A



BOTTOM SIDE DECOUPLING UNDER APU

Change +3VPCU to LDO3...Tommy0504

RTCVCC\_TP1

51225\_ID03

R133

1K\_5%\_4

R134

0.5%\_4

C99

0.22u/6.3V\_2

C100

1u/6.3V\_4

\*SOLDERJUMPER-2

Q10

2N7002K

R135

100K\_5%\_2

FPS

2150MHzFPS

U1P

POWER

Edward:25W CPU

G7

G10

G12

G14

G16

G18

G20

G22

G24

G26

G28

G30

G32

G34

G36

G38

G40

G42

G44

G46

G48

G50

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G582

G584

G586

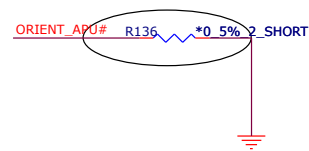
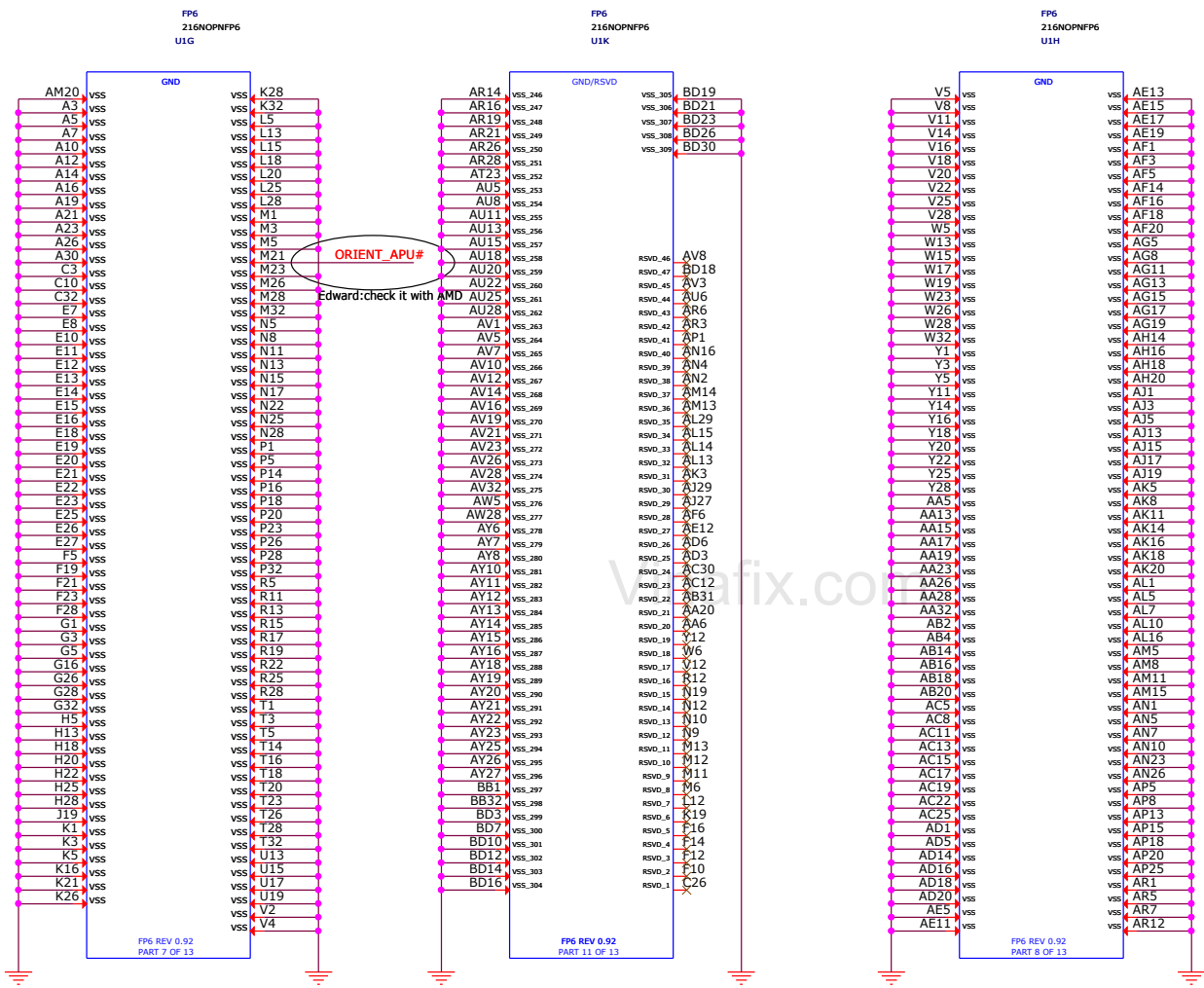
G588

G590

G592

G594





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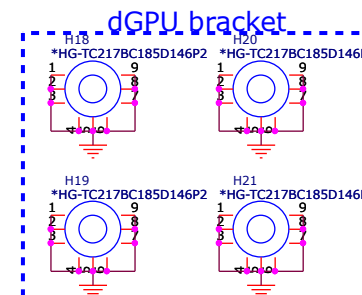
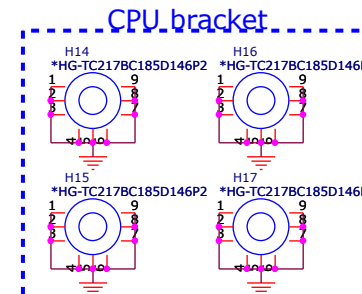
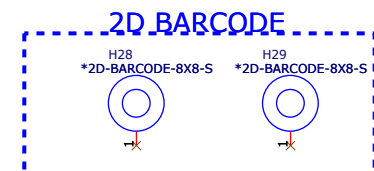
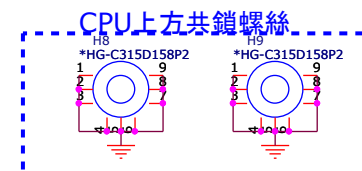
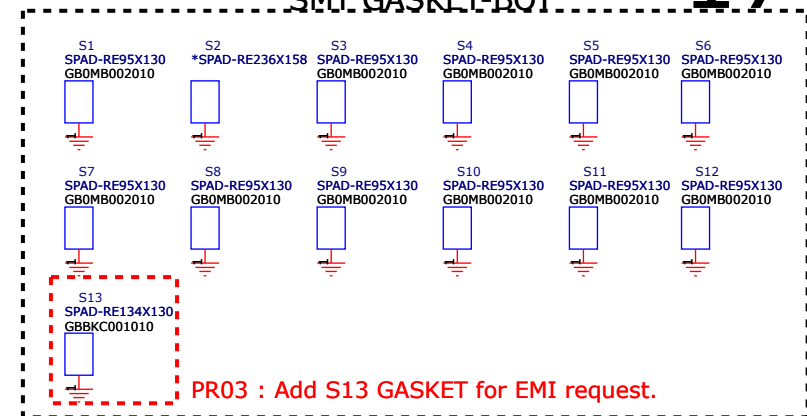
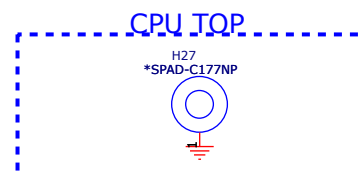
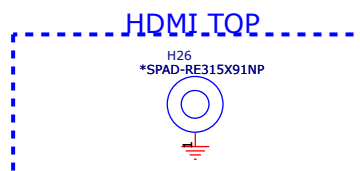
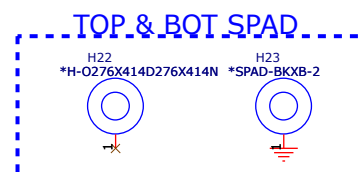
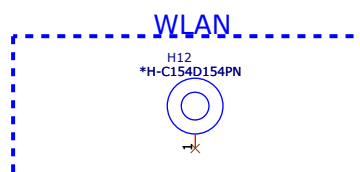
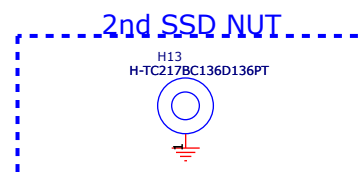
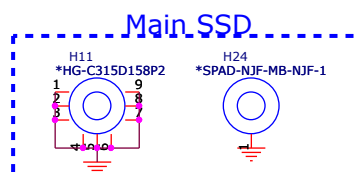
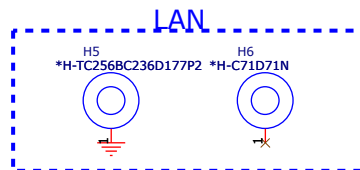
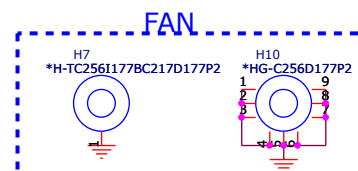
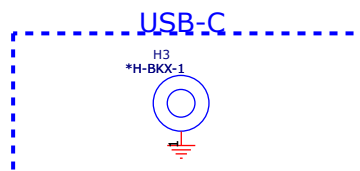
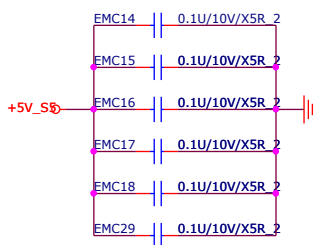
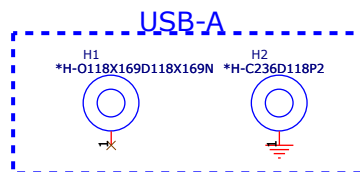
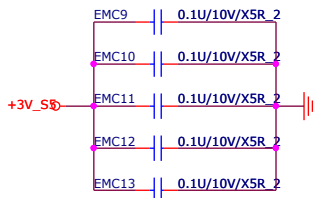
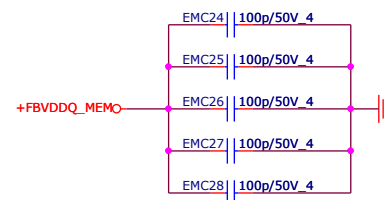
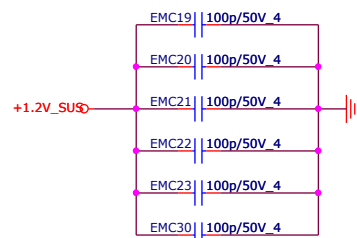
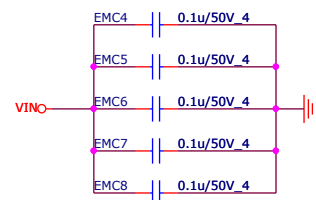
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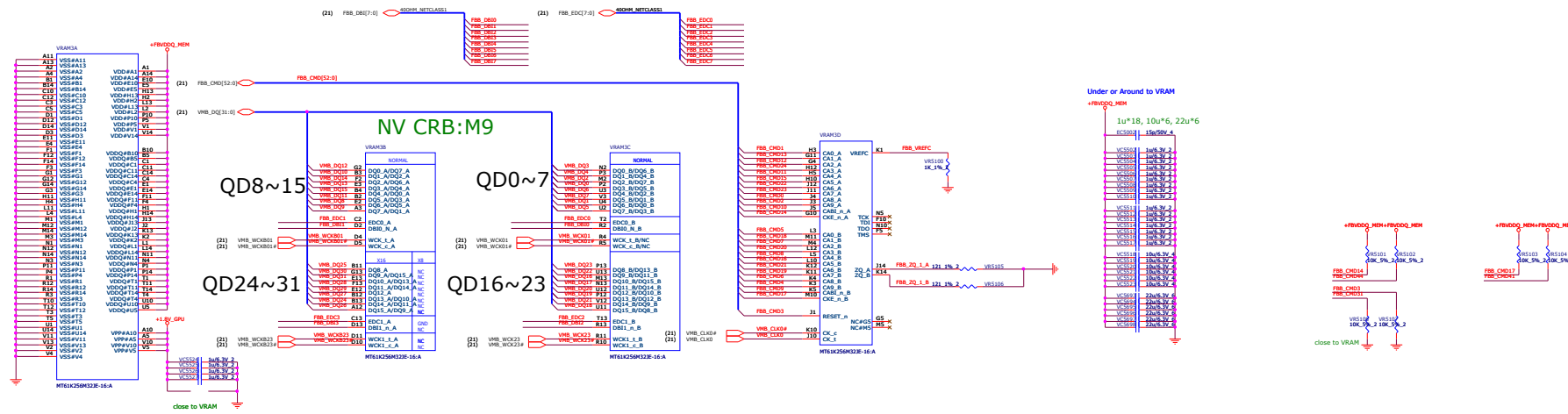




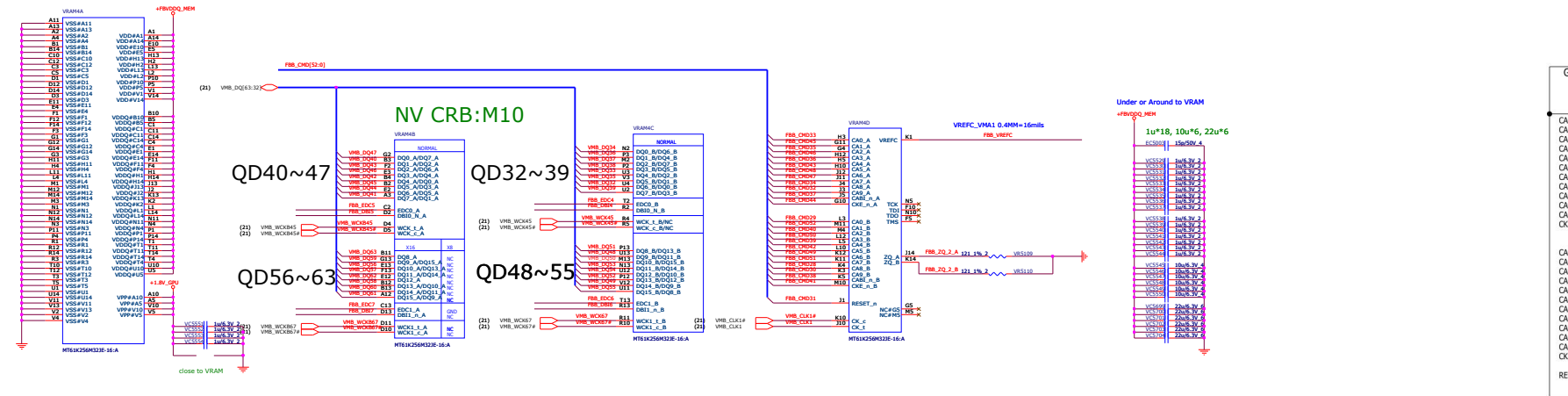








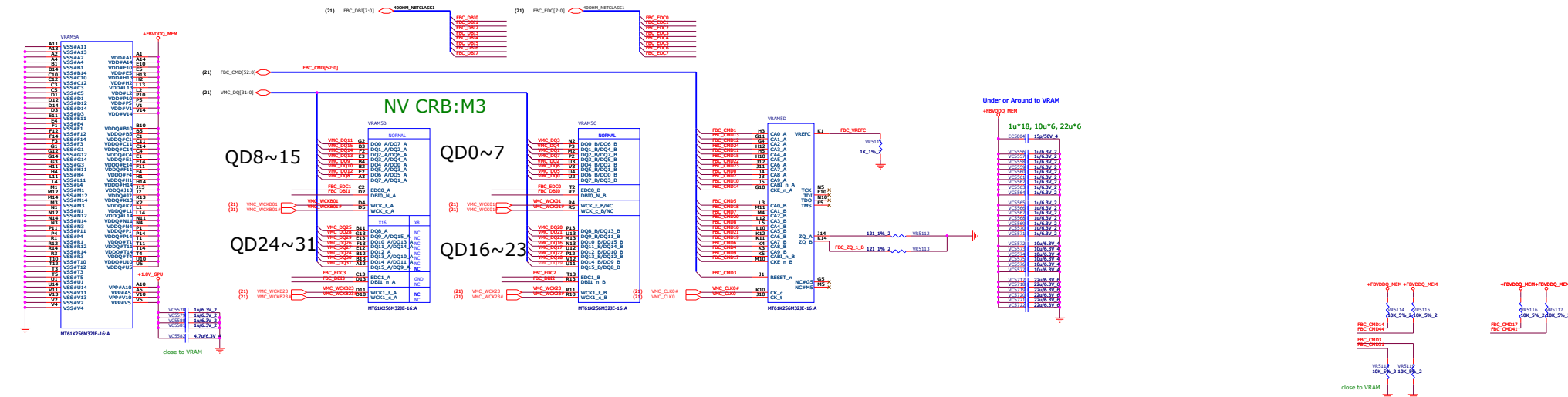
MEMORY: FBB Partition 63..32



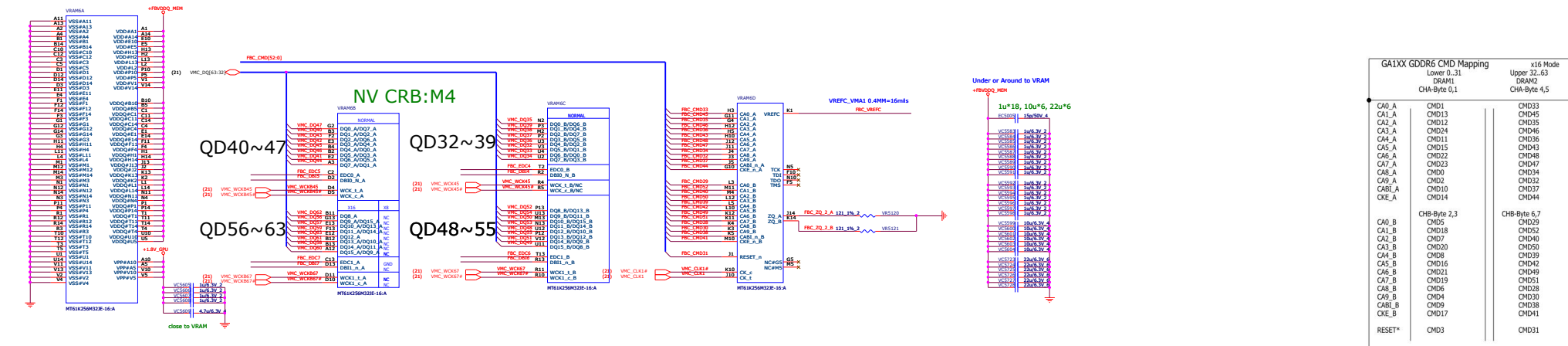
GA10X GDDR6s DMA Mapping		
	Lower 0.31 DRAM1 CHA-Byte 4,5	Upper 32.63 DRAM2 CHA-Byte 4,5
CA0_A	CM01	CM033
CA1_A	CM013	CM045
CA2_A	CM012	CM035
CA3_A	CM024	CM046
CA4_A	CM011	CM036
CA5_A	CM015	CM043
CA6_A	CM022	CM048
CA7_A	CM023	CM047
CA8_A	CM00	CM034
CA9_A	CM02	CM032
CAB_A	CM010	CM037
CCE_A	CM014	CM044
	CHB-Byte 2,3	CHB-Byte 5,6
CA0_B	CM05	CM029
CA1_B	CM018	CM052
CA2_B	CM07	CM040
CA3_B	CM020	CM050
CA4_B	CM08	CM039
CA5_B	CM016	CM042
CA6_B	CM011	CM049
CA7_B	CM019	CM051
CA8_B	CM06	CM028
CA9_B	CM04	CM030
CAB_B	CM09	CM048
CCE_B	CM017	CM041
RESET*	CM03	CM031



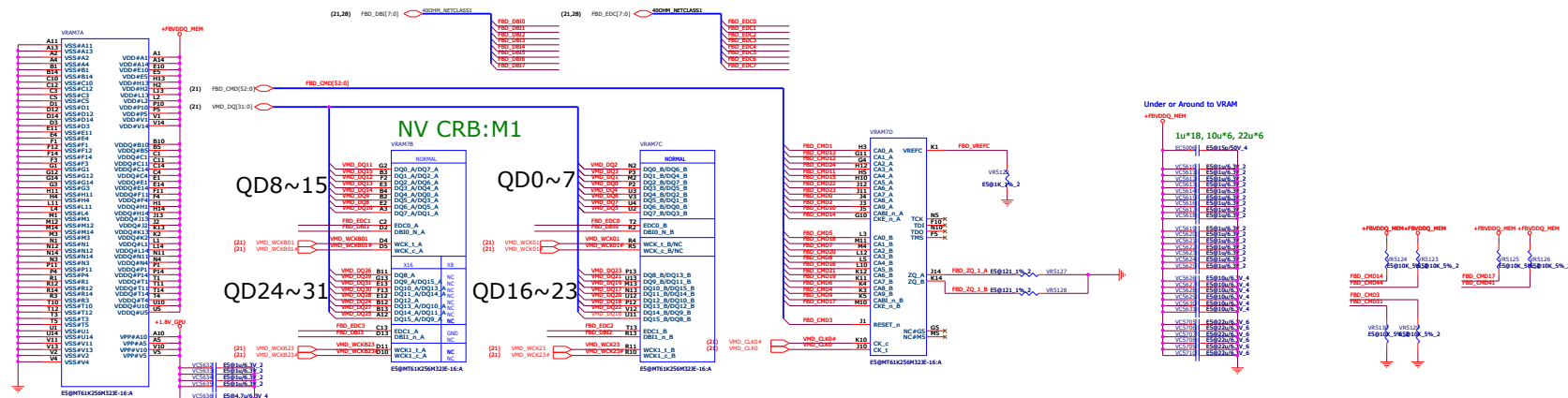
## MEMORY: FBC Partition 31..0



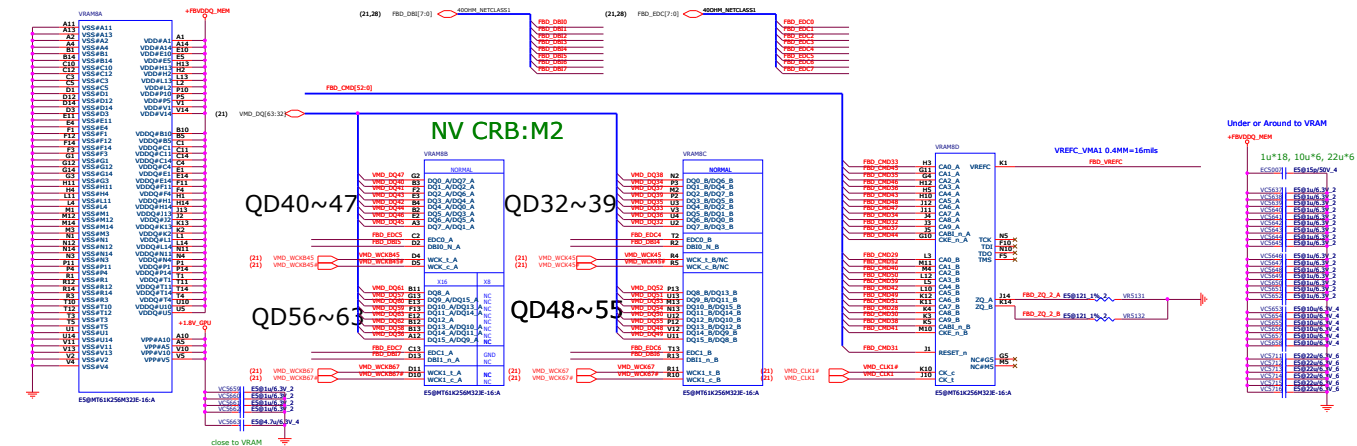
## MEMORY: FBC Partition 63..32



GAIXX GDDR6 CMD Mapping		x16 Mode	
		Lower 0..31	Upper 32..63
		DRAM2	DRAM2
		CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD0	CMD33	CMD45
CA1_A	CMD13	CMD45	CMD45
CA2_A	CMD13	CMD45	CMD45
CA3_A	CMD14	CMD46	CMD46
CA4_A	CMD11	CMD36	CMD36
CAS_A	CMD15	CMD43	CMD43
CAS_B	CMD22	CMD48	CMD48
CA7_A	CMD23	CMD47	CMD47
CAB_A	CMD0	CMD34	CMD34
CAB_B	CMD2	CMD32	CMD32
CAB_C	CMD10	CMD37	CMD37
CAB_D	CMD14	CMD44	CMD44
CHB-Byte 2,3		CHB-Byte 6,7	CHB-Byte 6,7
CA0_B	CMD5	CMD29	CMD29
CA1_B	CMD18	CMD52	CMD52
CA2_B	CMD17	CMD51	CMD51
CA3_B	CMD20	CMD50	CMD50
CA4_B	CMD8	CMD39	CMD39
CAS_B	CMD16	CMD42	CMD42
CAB_C	CMD19	CMD49	CMD49
CA7_B	CMD21	CMD51	CMD51
CAB_D	CMD28	CMD58	CMD58
CAB_E	CMD4	CMD30	CMD30
CAB_F	CMD9	CMD38	CMD38
CAB_G	CMD17	CMD41	CMD41
RESET*	CMD3	CMD31	CMD31

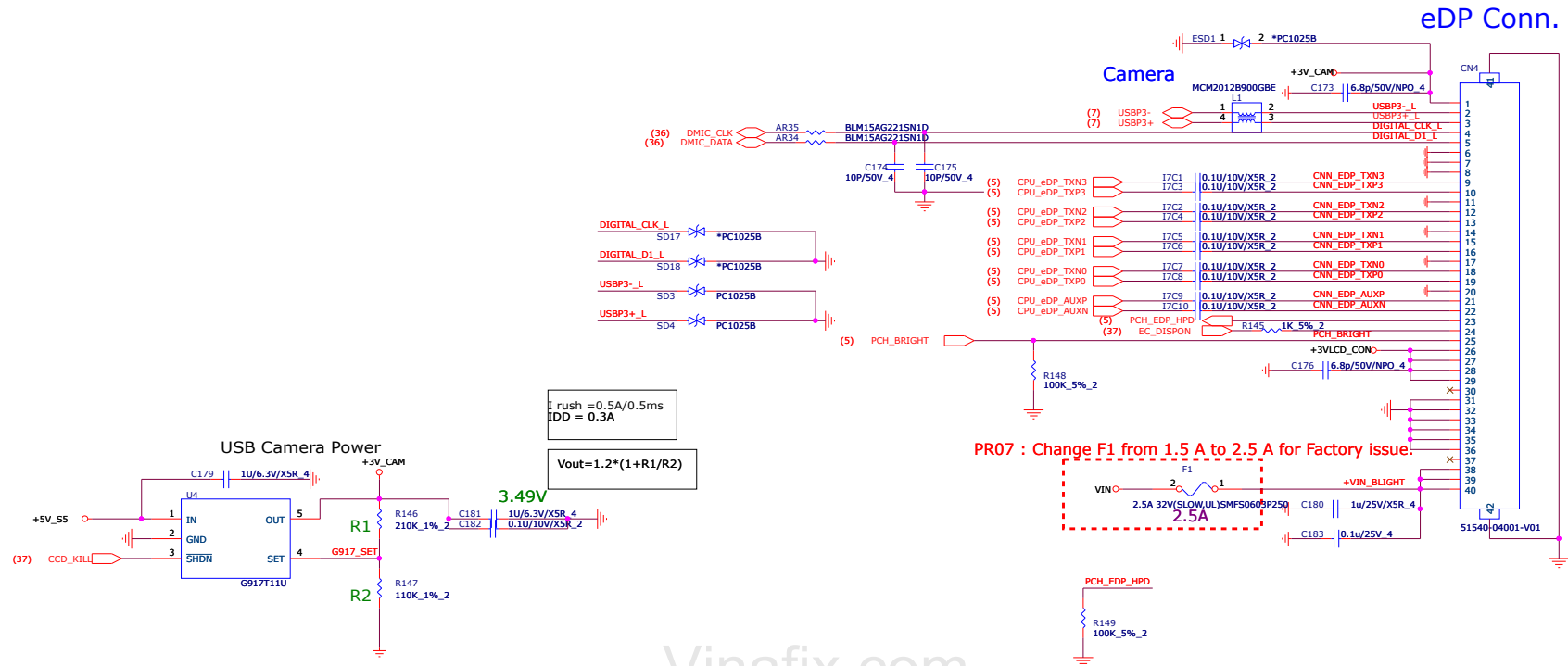


MEMORY: FBD Partition 63..32



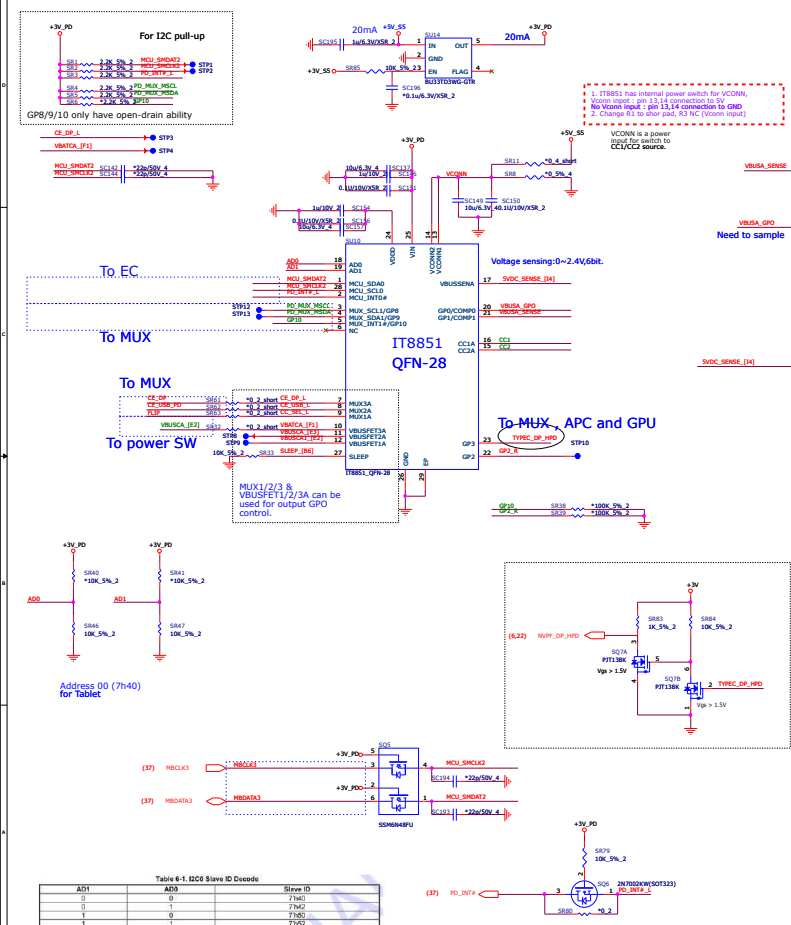
GA11X GDDR6 CMD Mapping		x16 Mode
Lower 0.31		Upper 32..63
DRAM1		DRAM2
CHB-Byte 0,1		CHB-Byte 4,5
CAL0_A	CM01	CM033
CAL1_A	CM10	CM045
CAL2_A	CM12	CM057
CAL3_A	CM24	CM046
CAL4_A	CM11	CM036
CAL5_A	CM15	CM043
CAL6_A	CM22	CM048
CAL7_A	CM13	CM047
CAE0	CM00	CM034
CAB0_A	CM02	CM032
CAB1_A	CM10	CM037
CKE_A	CM14	CM044
	CHB-Byte 2,3	CHB-Byte 6,7
CAE5	CM05	CM039
CAL1_B	CM18	CM052
CAL2_B	CM07	CM040
CAL3_B	CM20	CM050
CAL4_B	CM08	CM039
CAL5_B	CM16	CM042
CAL6_B	CM21	CM049
CAL7_B	CM19	CM051
CAB0_B	CM09	CM028
CAB1_B	CM17	CM030
CKE_B	CM09	CM041
RESET**	CM03	CM031



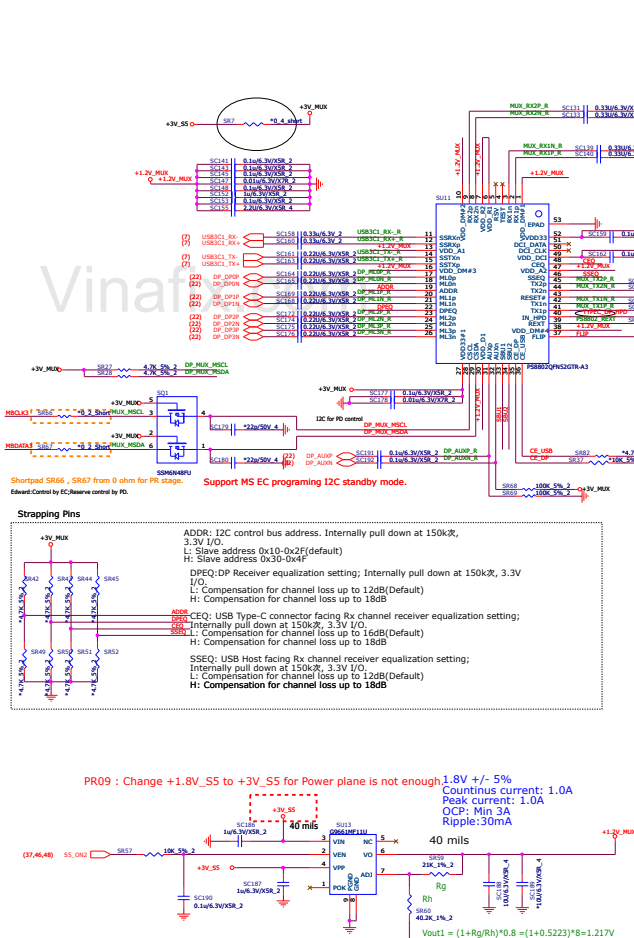


ER08 : Reserved SD22 for ESD request .

# PD Controller

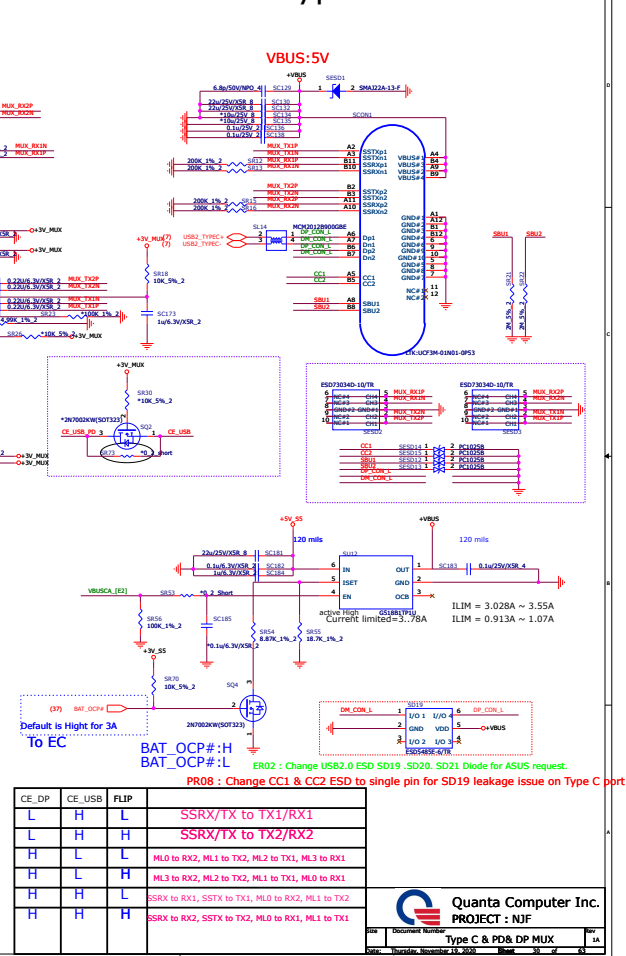


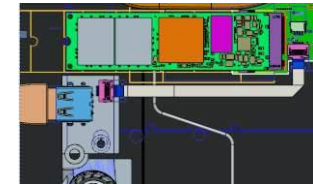
# DP MUX



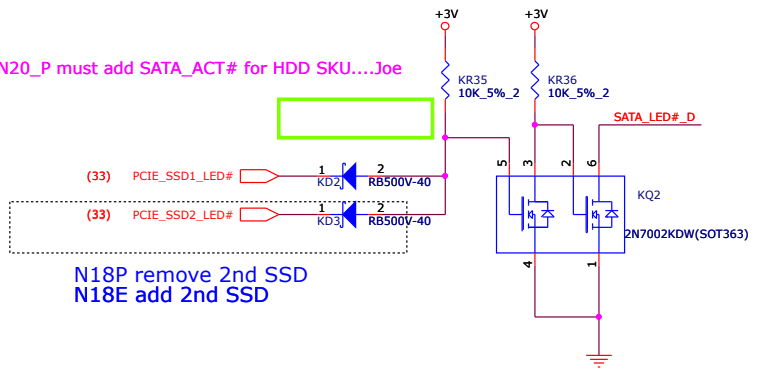
# Type C

# 30

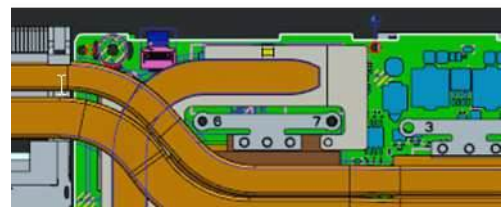
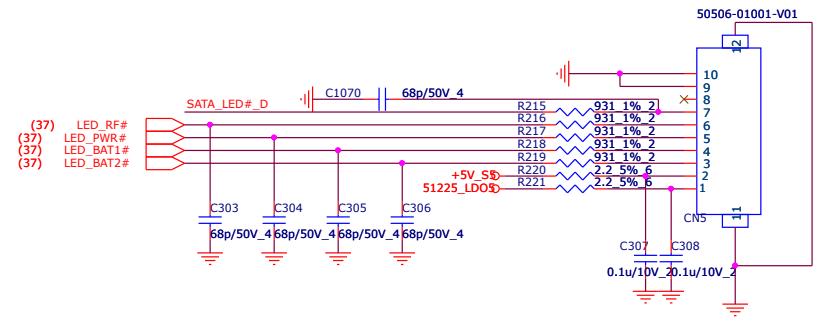




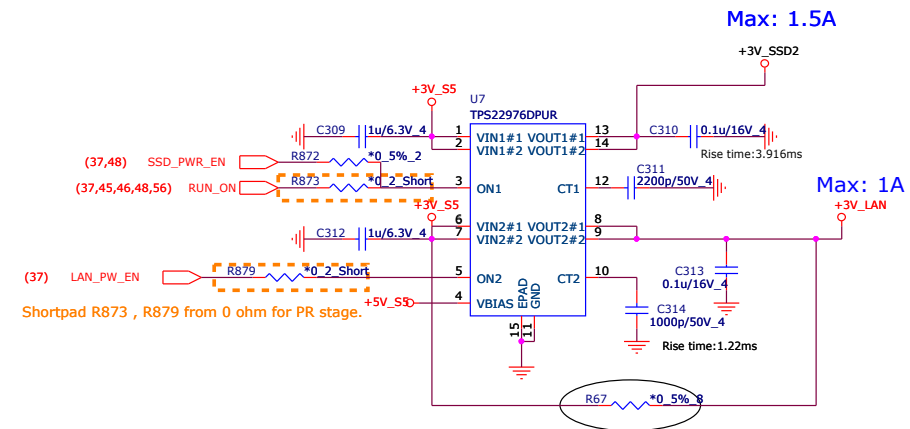
GN20\_P must add SATA\_ACT# for HDD SKU....Joe



N18P remove 2nd SSD  
N18E add 2nd SSD



Vinafix.com





Vinafix.com

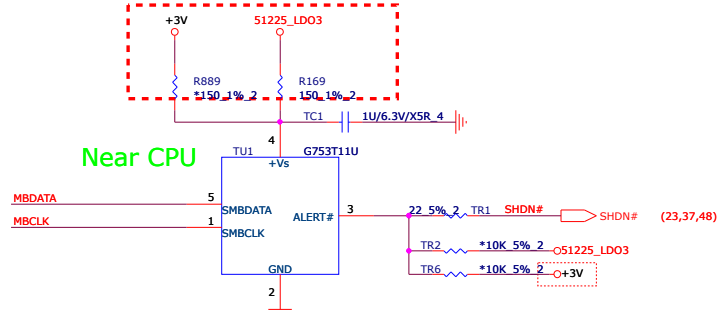


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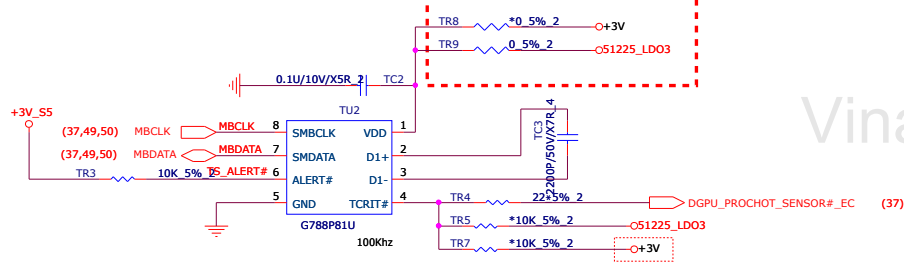
# Thermal

PR12 :Change TU1 power rail from 51225\_LDO3 to +3V for power consumption under 0.4mA on battery mode.

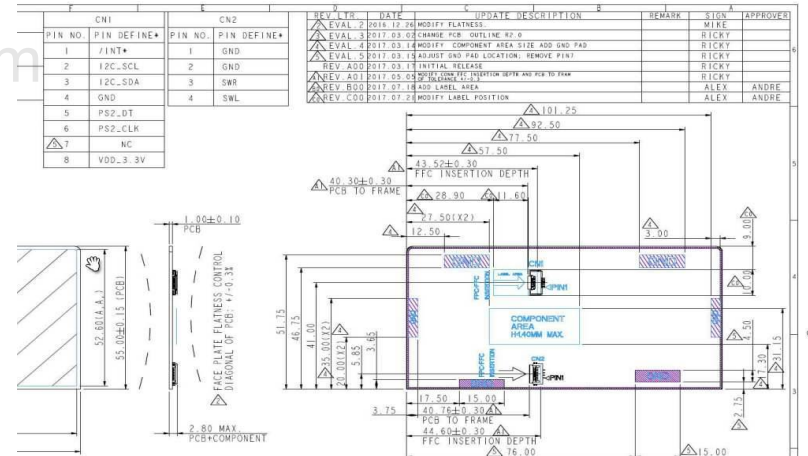
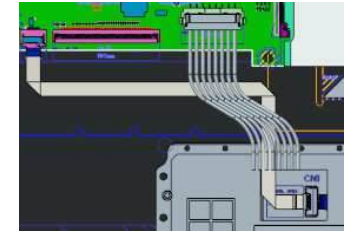
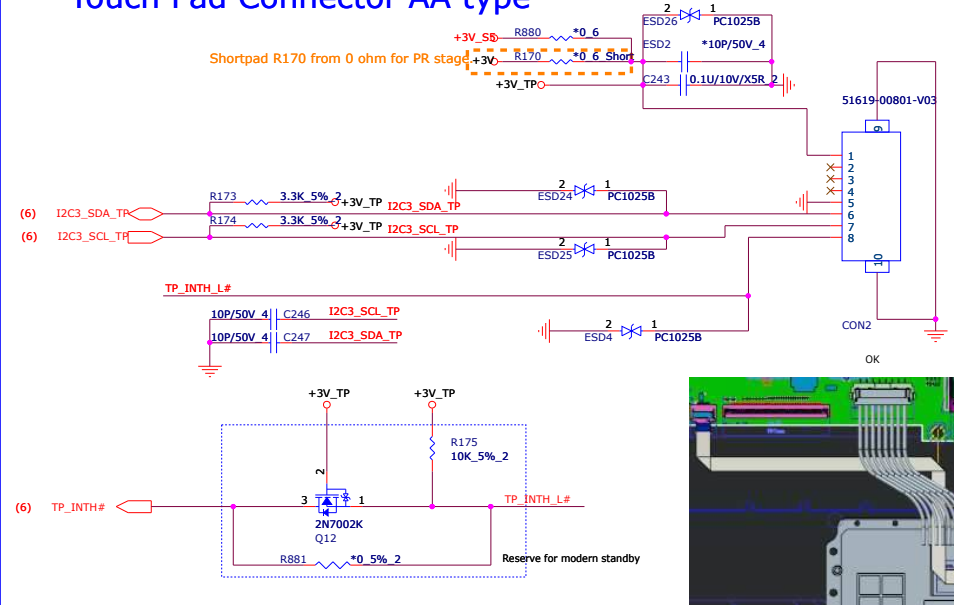


MP02 : Change TU1 and TU2 power rail from +3V to 51225\_LDO3

PR13 :Change TU2 power rail from 51225\_LDO3 to +3V for power consumption under 0.4mA on battery mode.

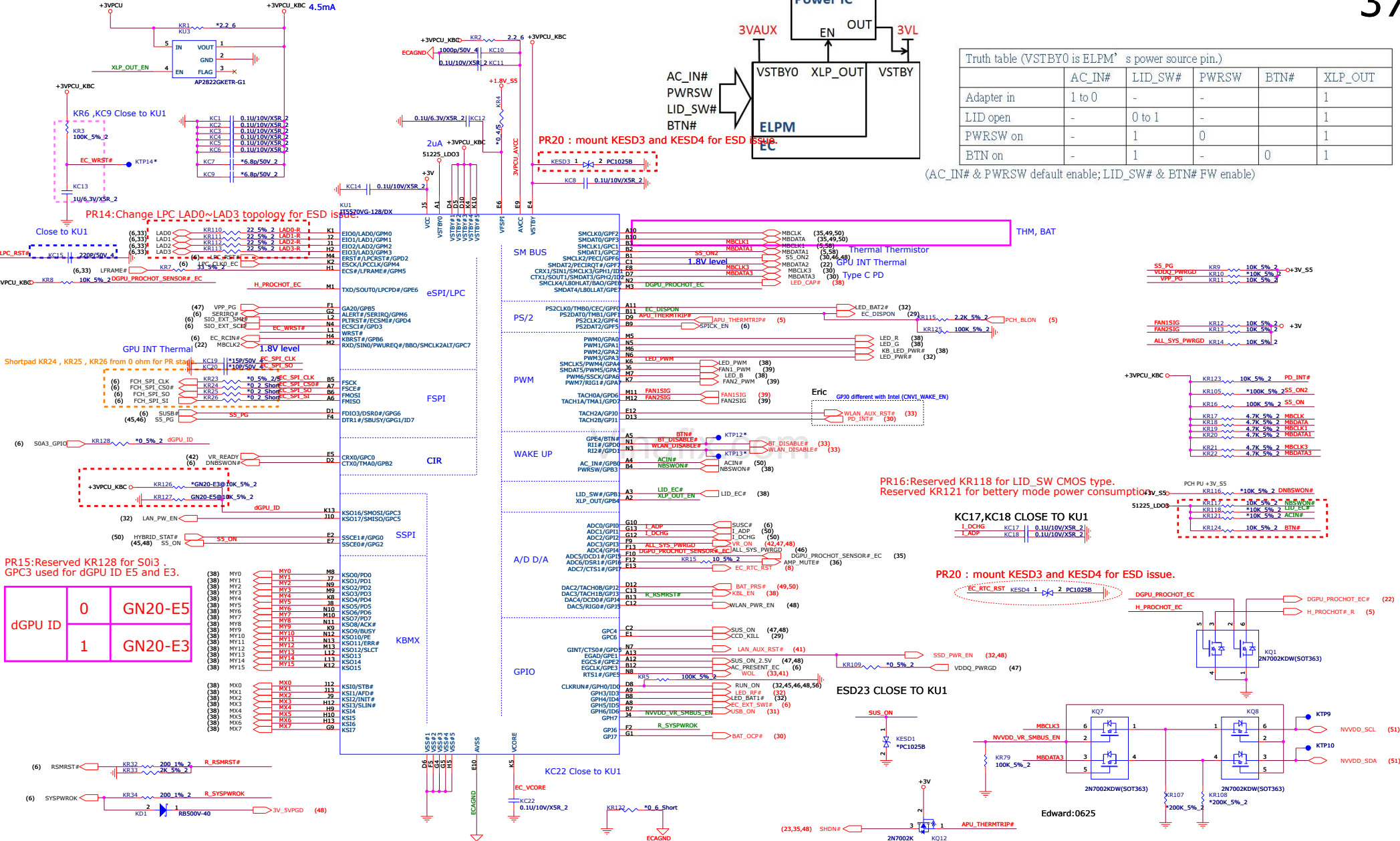


# Touch Pad Connector AA type









Truth table (VSTBY0 is ELPM's power source pin.)

	AC_IN#	LID_SW#	PWRSW	BTN#	XLP_OUT
Adapter in	1 to 0	-	-	-	1
LID open	-	0 to 1	-	-	1
PWRSW on	-	1	0	-	1
BTN on	-	1	-	0	1

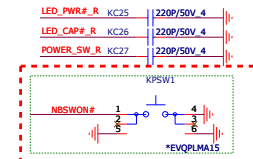
(AC\_IN# & PWRSW default enable; LID\_SW# & BTN# FW enable)

PR15: Reserved KR128 for S0I3 .  
GPC3 used for dGPU ID E5 and E3.

dGPU ID	
0	GN20-E5
1	GN20-E3

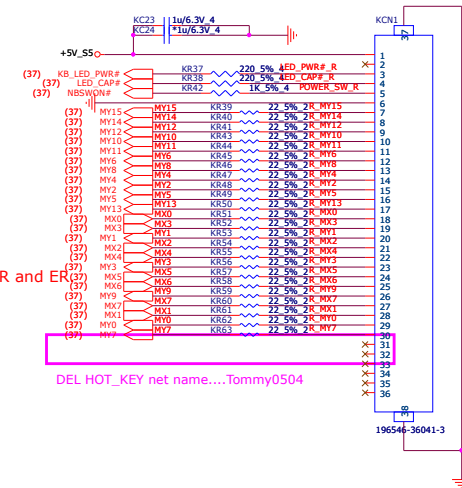
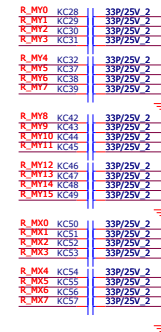
PR16: Reserved KR118 for LID\_SW CMOS type.  
Reserved KR121 for battery mode power consumption.

PR20 : mount KESD3 and KESD4 for ESD issue.

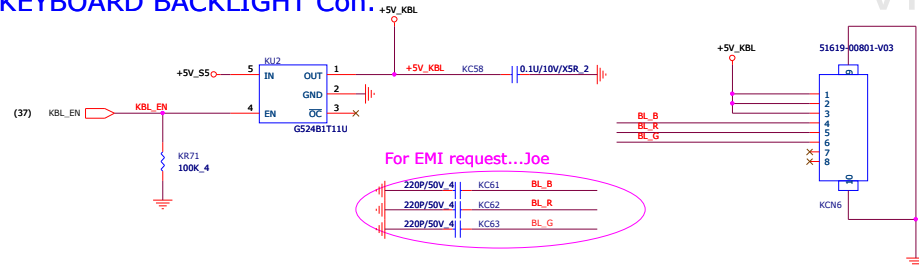


Reserve PSW1 for SR/ER debug

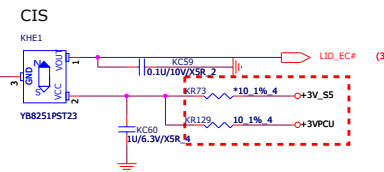
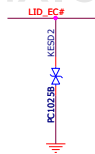
PRI7 : un-mount KPSW1 , only debug for SR and ER



## KEYBOARD BACKLIGHT Con.



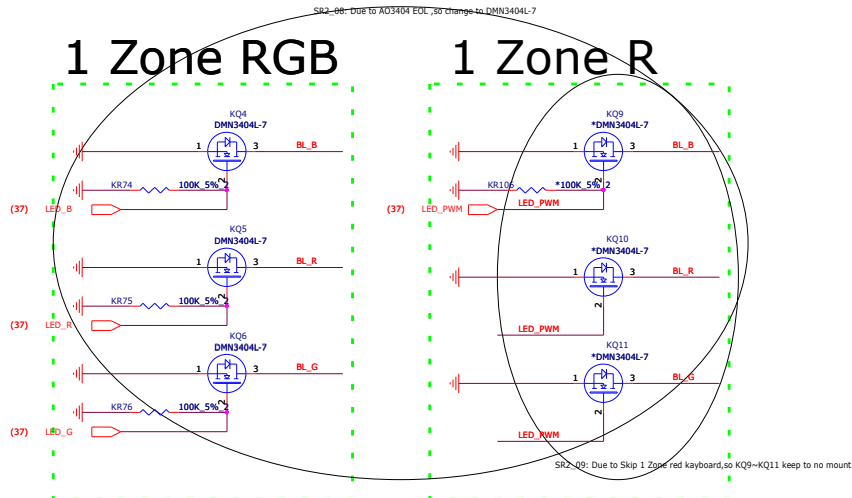
ESD23 CLOSE TO KHE1

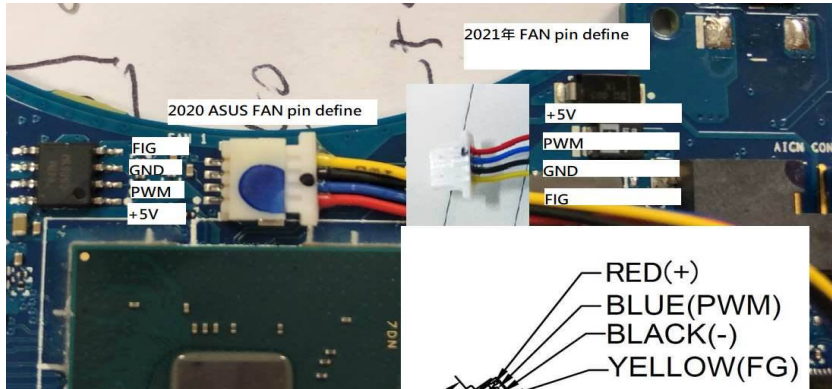


PR18 : Change KHE1 power rail from +3VPCU to +3V\_S5 for power consumption under 0.4mA on battery mode .  
MP03 : Add KHE1 power rail from +3V\_S5 to +3V\_PCU.

## 1 Zone RGB

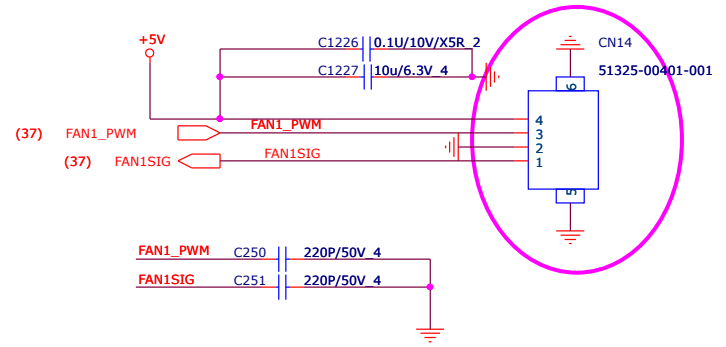
## 1 Zone R





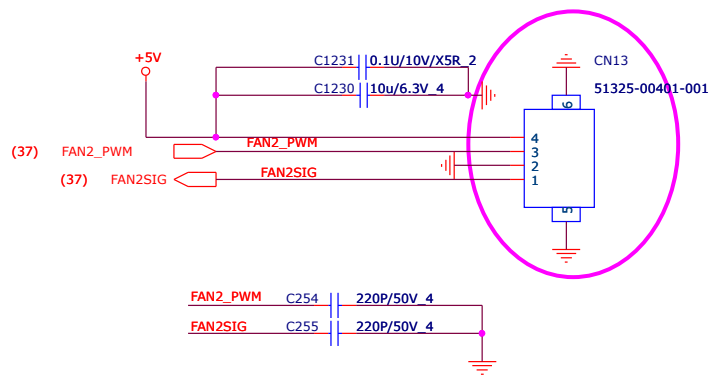
# FAN1 for CPU

Add +12V power rail and change CAP to 25V...Tommy0504



ER07 : Change FAN connector from 5-pin to 4-pin for CN13 and CN14 .

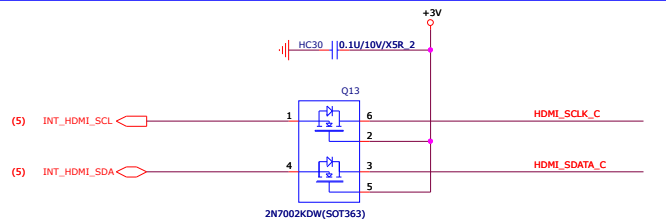
# FAN2 for GPU



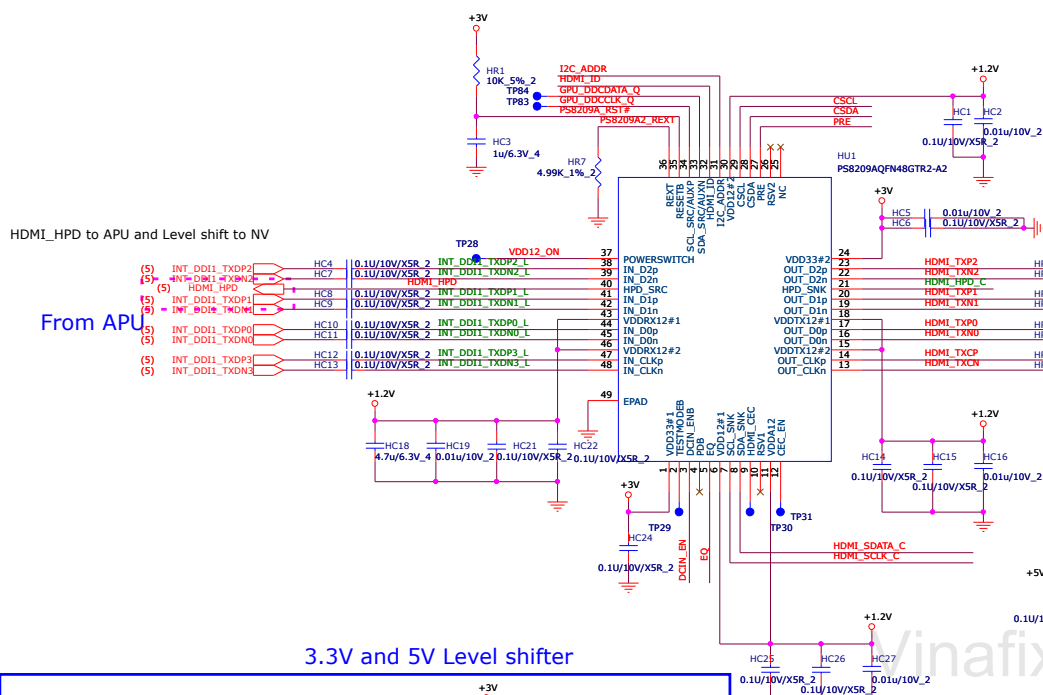
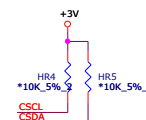
HDMI\_HPDI to APU and Level shift to NV

From APU

3.3V and 5V Level shifter



Optional



For HDMI2.1 Inter-pair skew...Joe

Near CON side

Near CON side

Near CON side

Near CON side

Near CON side

Near CON side

Near CON side

Near CON side

Near CON side

Near CON side

Near CON side

Near CON side

Near CON side

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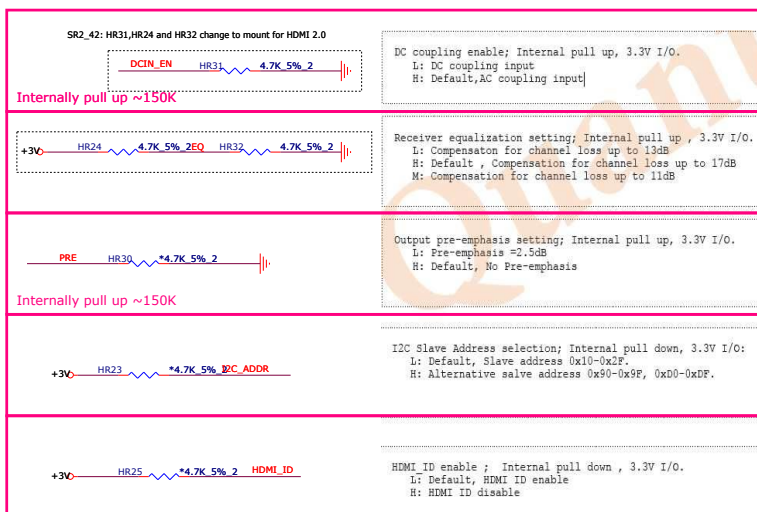
Near CON side

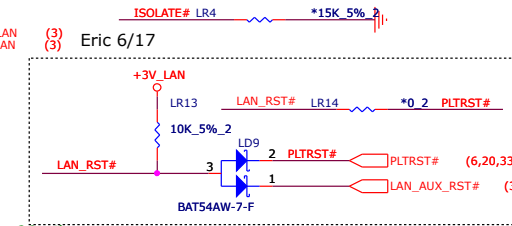
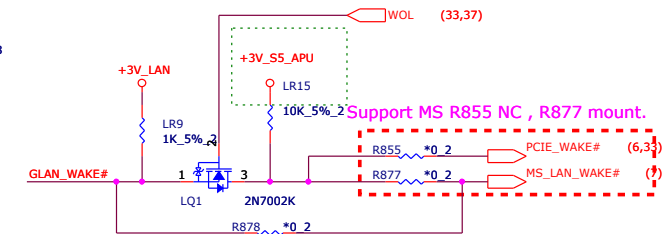
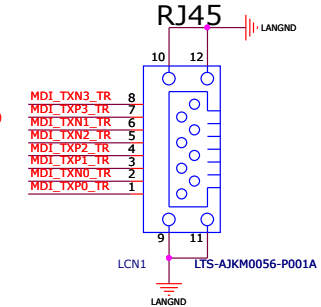
Near CON side

Near CON side

Near CON side

Near CON side




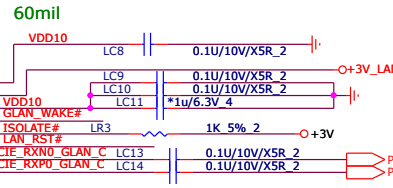
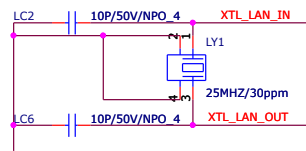
LAN CONN

PR19 : Reserved R855 for power management by customer's table list.

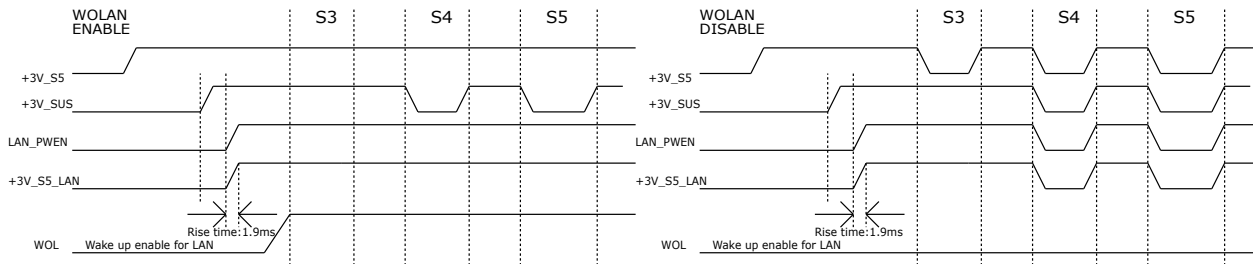
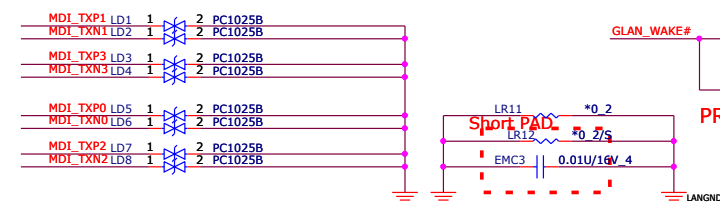
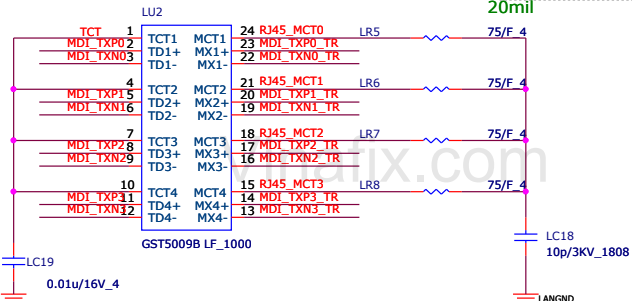
AC Mode : Support wake on LAN  
DC Mode : Don't support wake on LAN

BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	L	L

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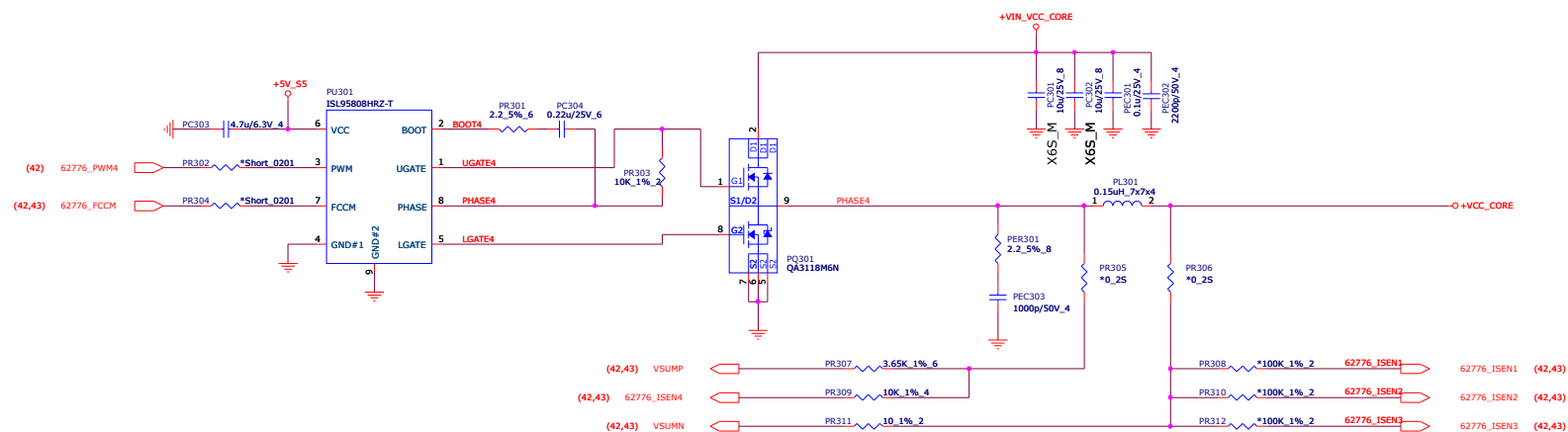
LU1: +3V\_S5\_LAN Rise time > 0.5ms



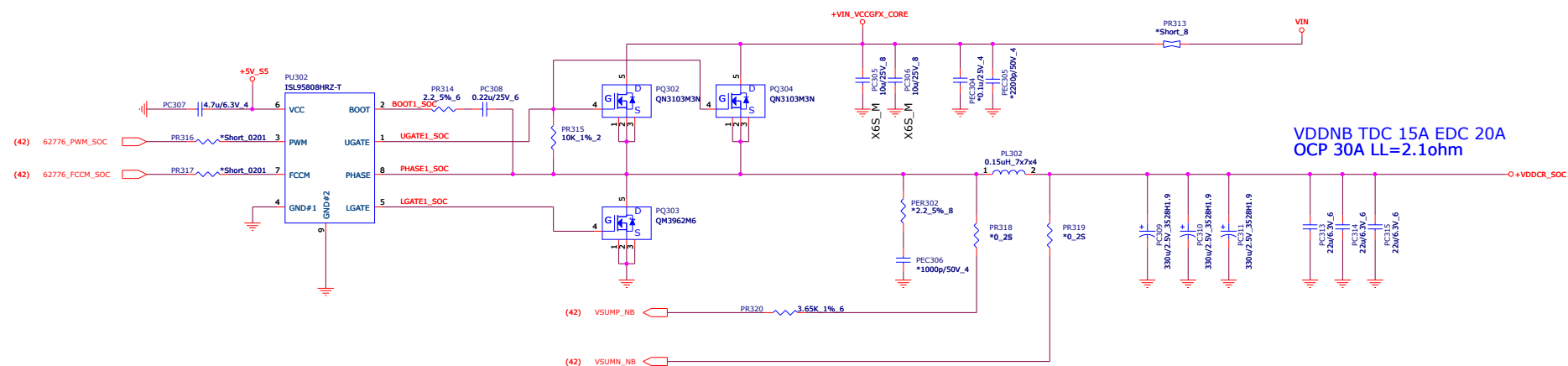




## VCORE Phase4

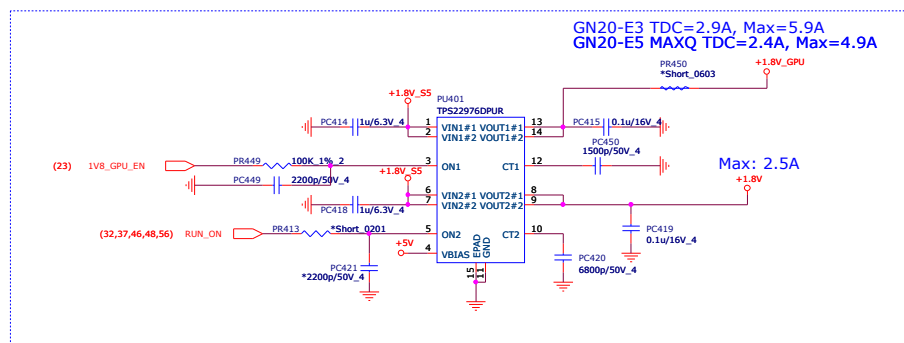
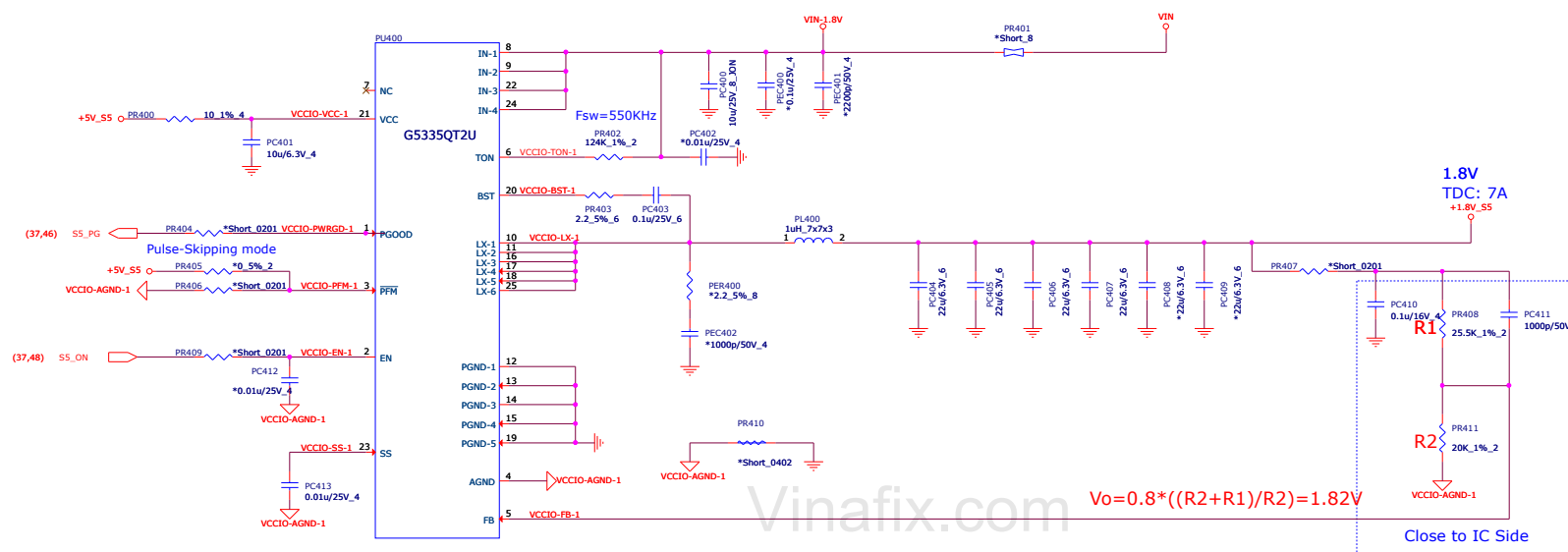


## VDDCR\_SOC

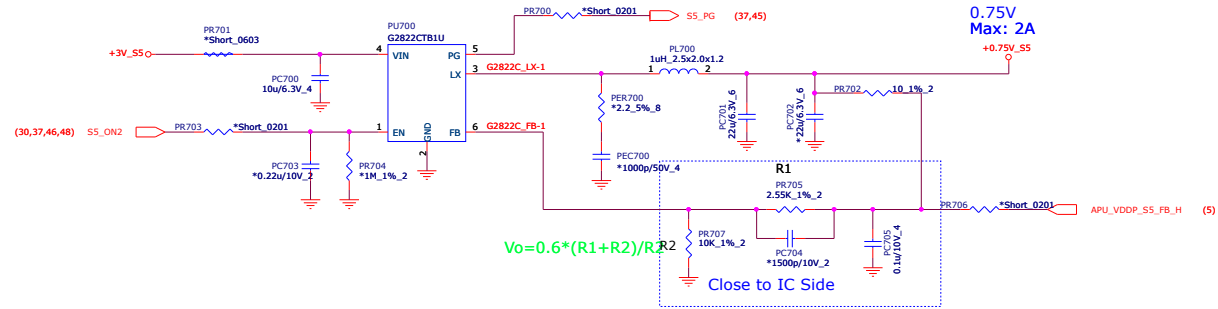




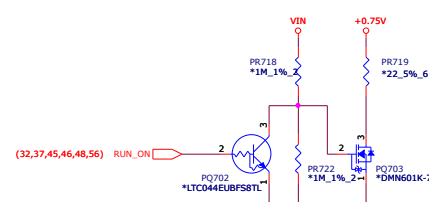
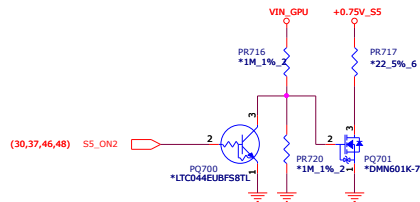
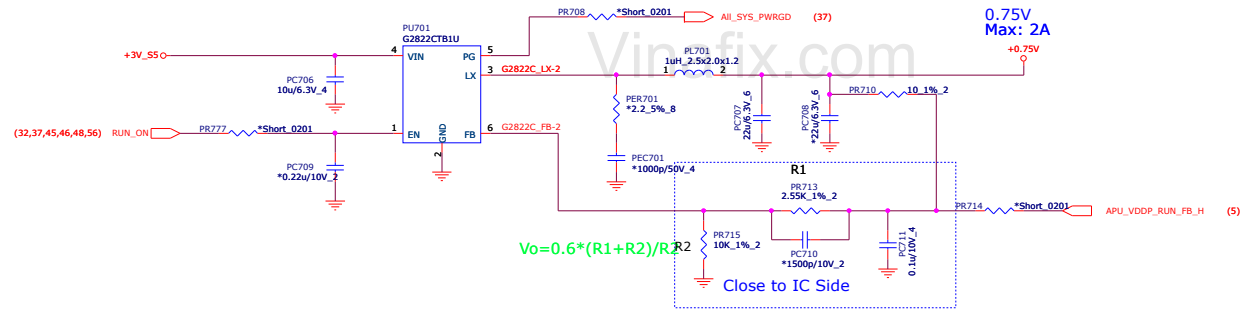
## +1.8V\_S5



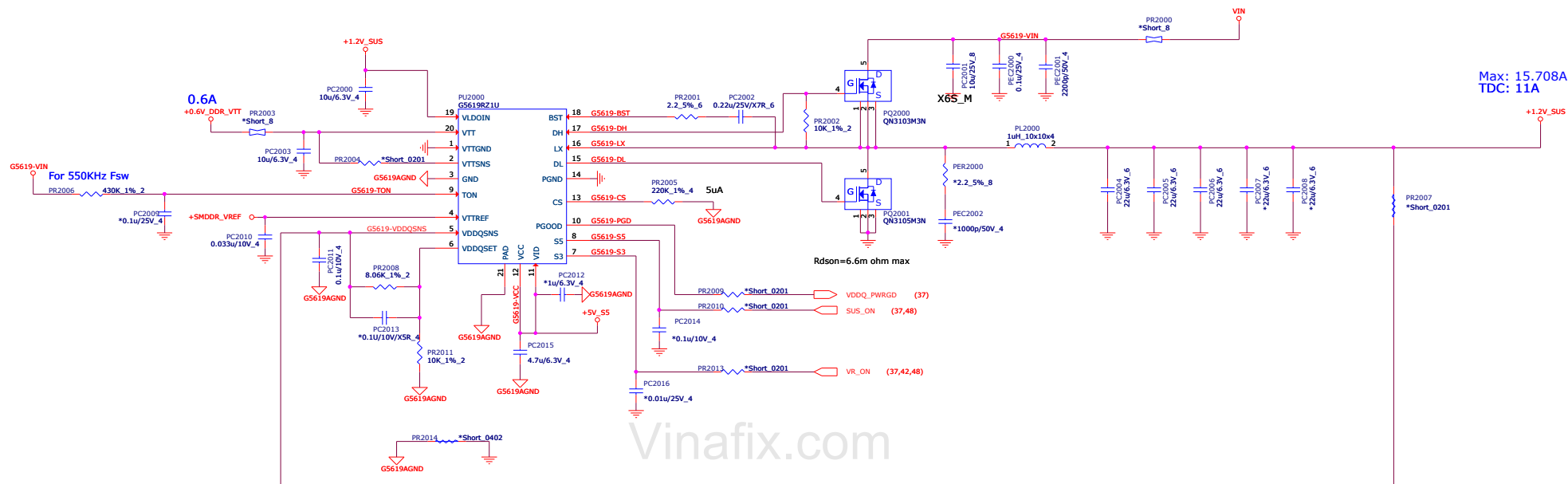
## +0.75V\_S5



## +0.75V

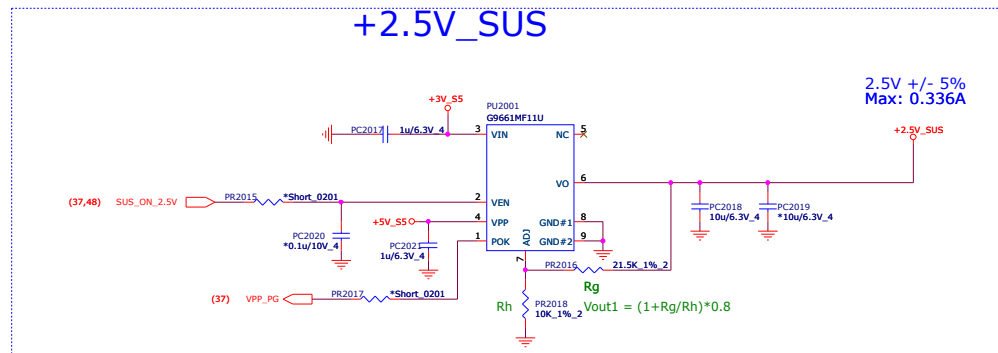


## 1.2VSUS &amp; VTT\_MEM



STATE	S3	S5	+1.2V_SUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

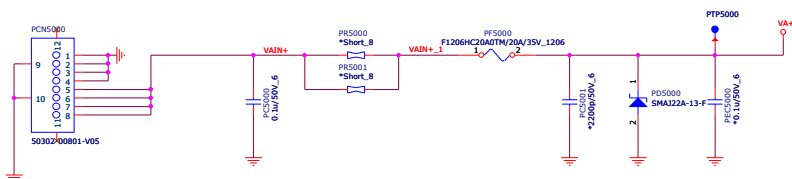
## +2.5V\_SUS





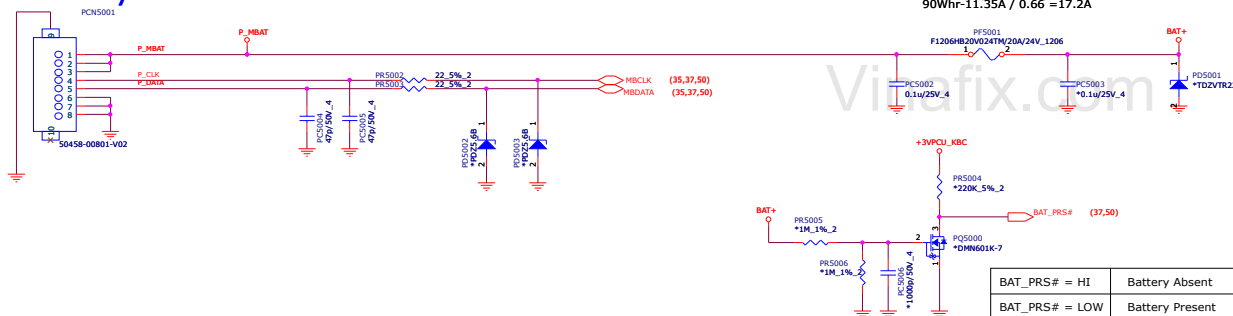
## AC IN (On-Board DC-Jack)

Fuse Rating =  
 $IR(max) / (0.75 * 0.88)$   
 $200W/20V / 0.66 = 15.15A$

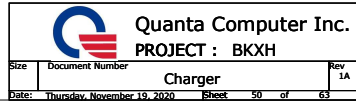


## Battery IN

Fuse Rating =  
 $IR(max) / (0.75 * 0.88)$   
 $90Whr-11.35A / 0.66 = 17.2A$



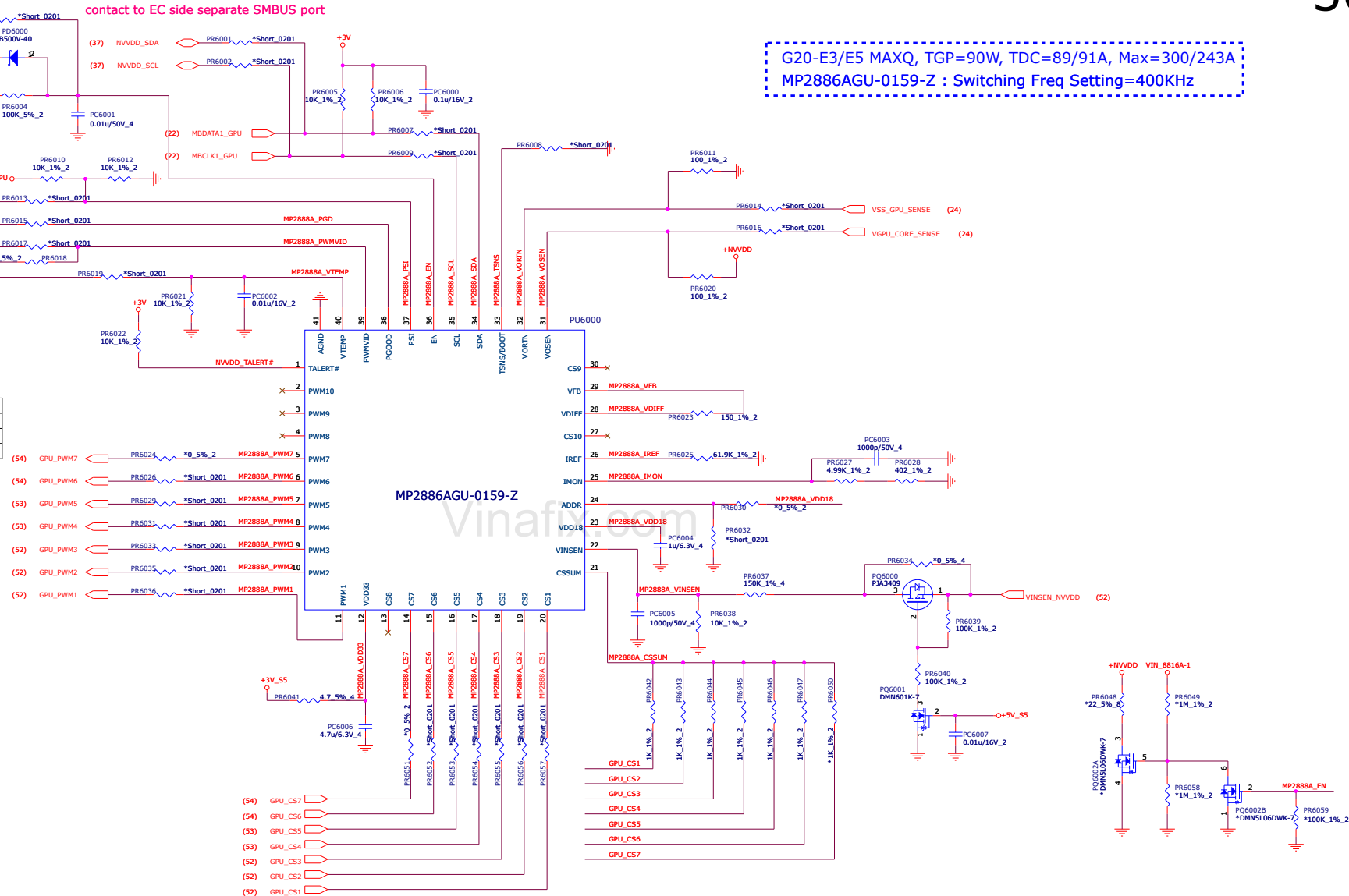
BAT_PR# = HI	Battery Absent
BAT_PR# = LOW	Battery Present



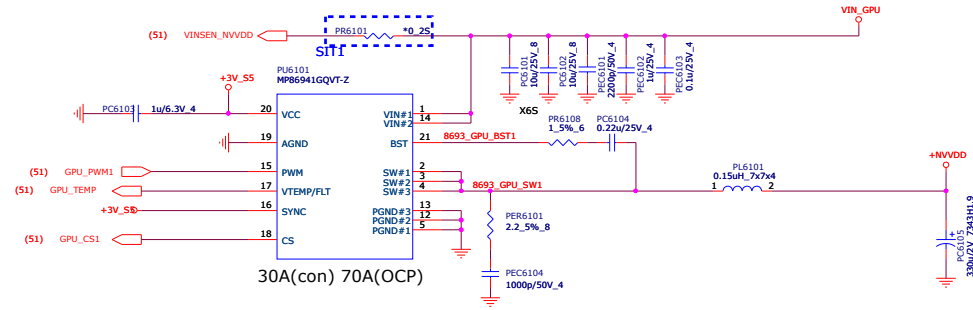
contact to EC side separate SMBUS port

G20-E3/E5 MAXQ, TGP=90W, TDC=89/91A, Max=300/243A  
MP2886AGU-0159-Z : Switching Freq Setting=400KHz

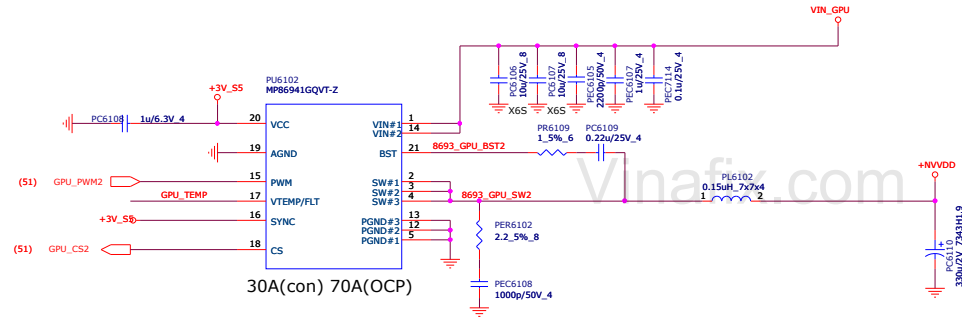
PSI	PWM Status
1	Forced CCM for all phases
0	Adjustable low phase count
Hi-Z	Auto phase-shedding enabled



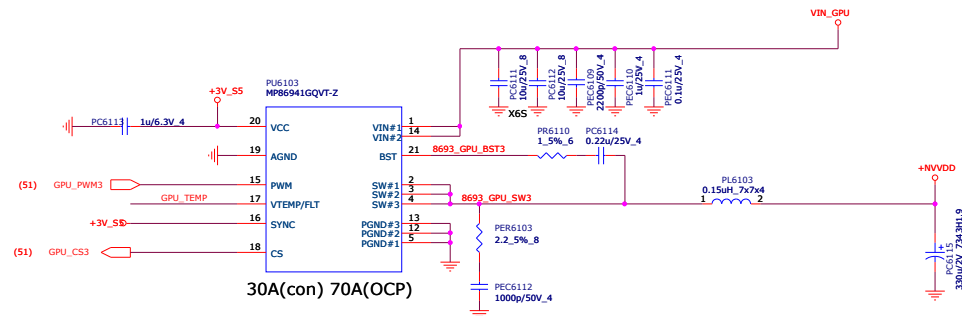
## NVVDD Phase-1



## NVVDD Phase-2

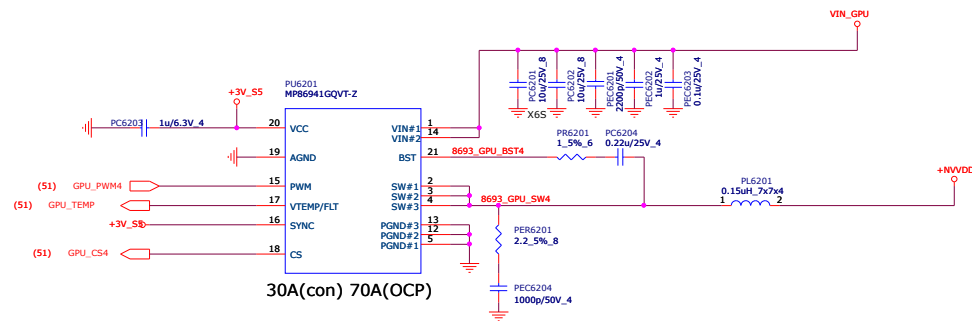


## NVVDD Phase-3

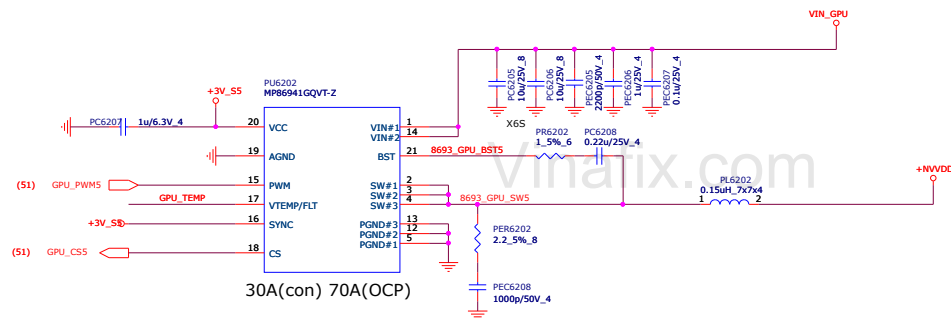




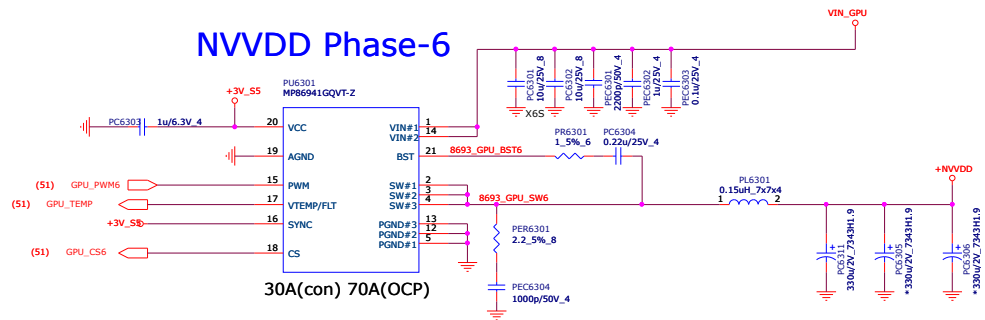
## NVVDD Phase-4



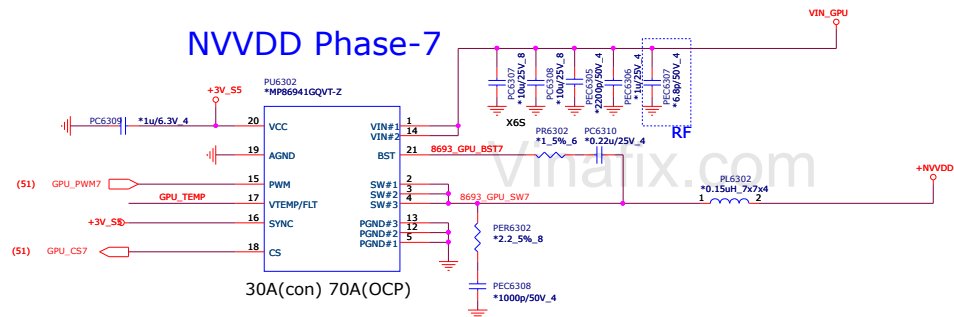
## NVVDD Phase-5



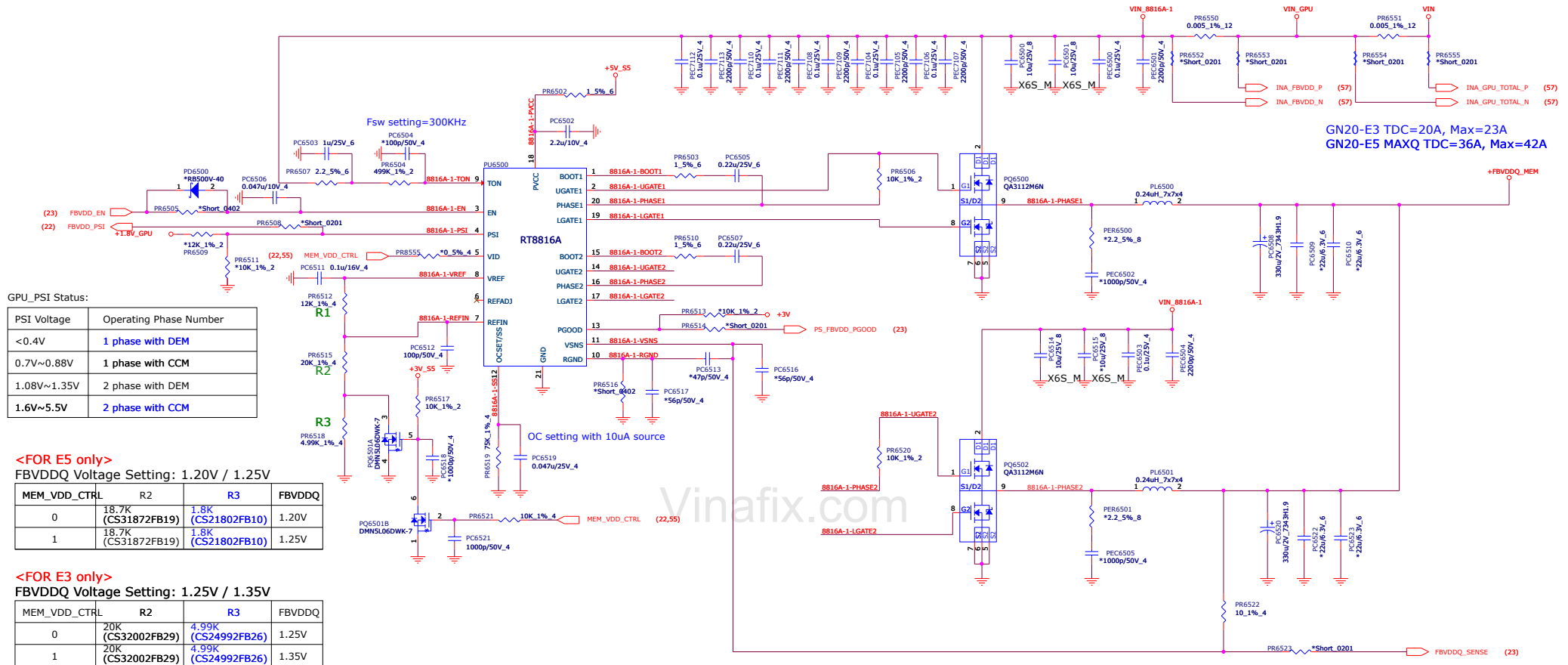
## NVVDD Phase-6



## NVVDD Phase-7

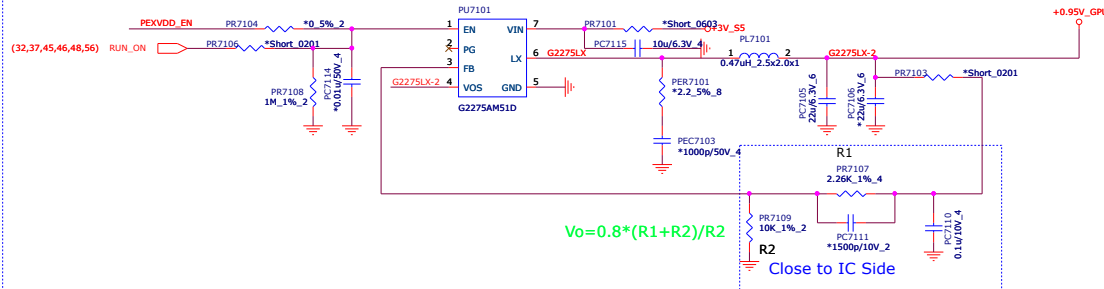


## +FBVDDQ\_MEM



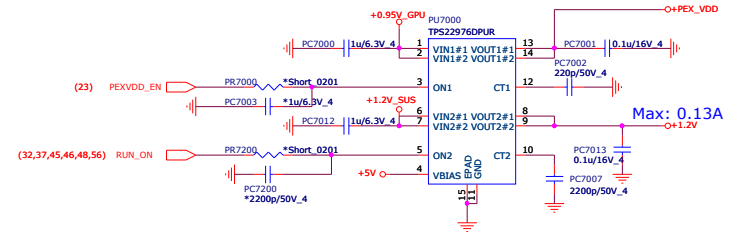
## +0.95V\_GPU

GN20-E3 TDC=2.1A, Max=4.2A  
GN20-E5 MAXQ TDC=2A, Max=4.1A



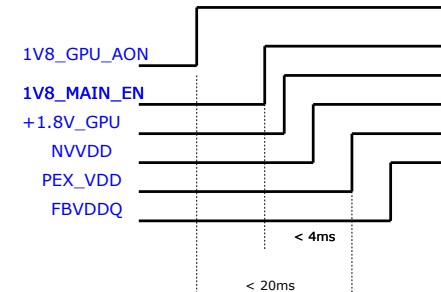
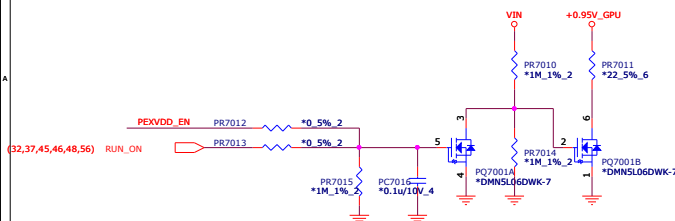
## Load Switch for GPU

GN20-E3 TDC=2.1A, Max=4.2A  
GN20-E5 MAXQ TDC=2A, Max=4.1A

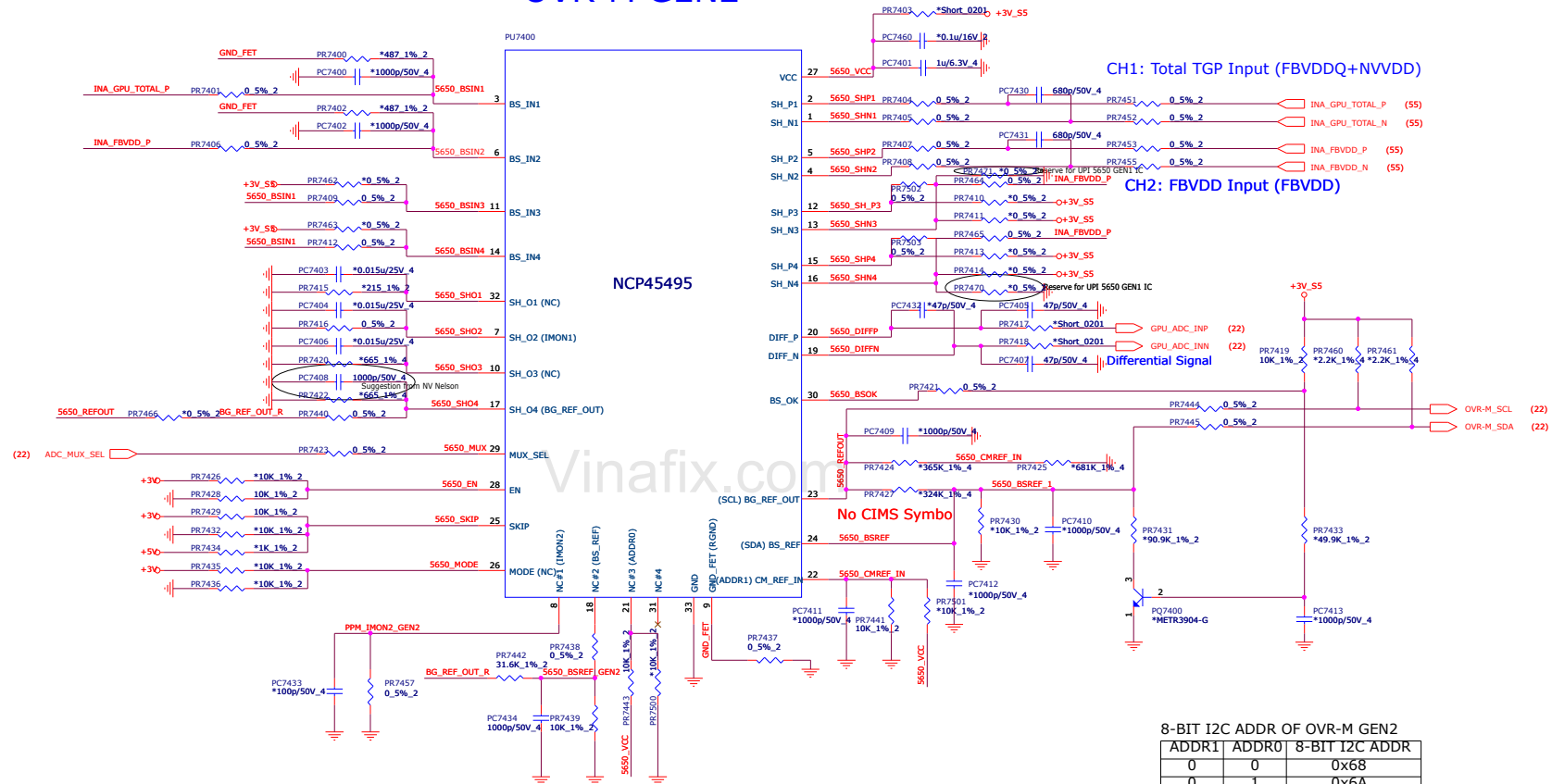


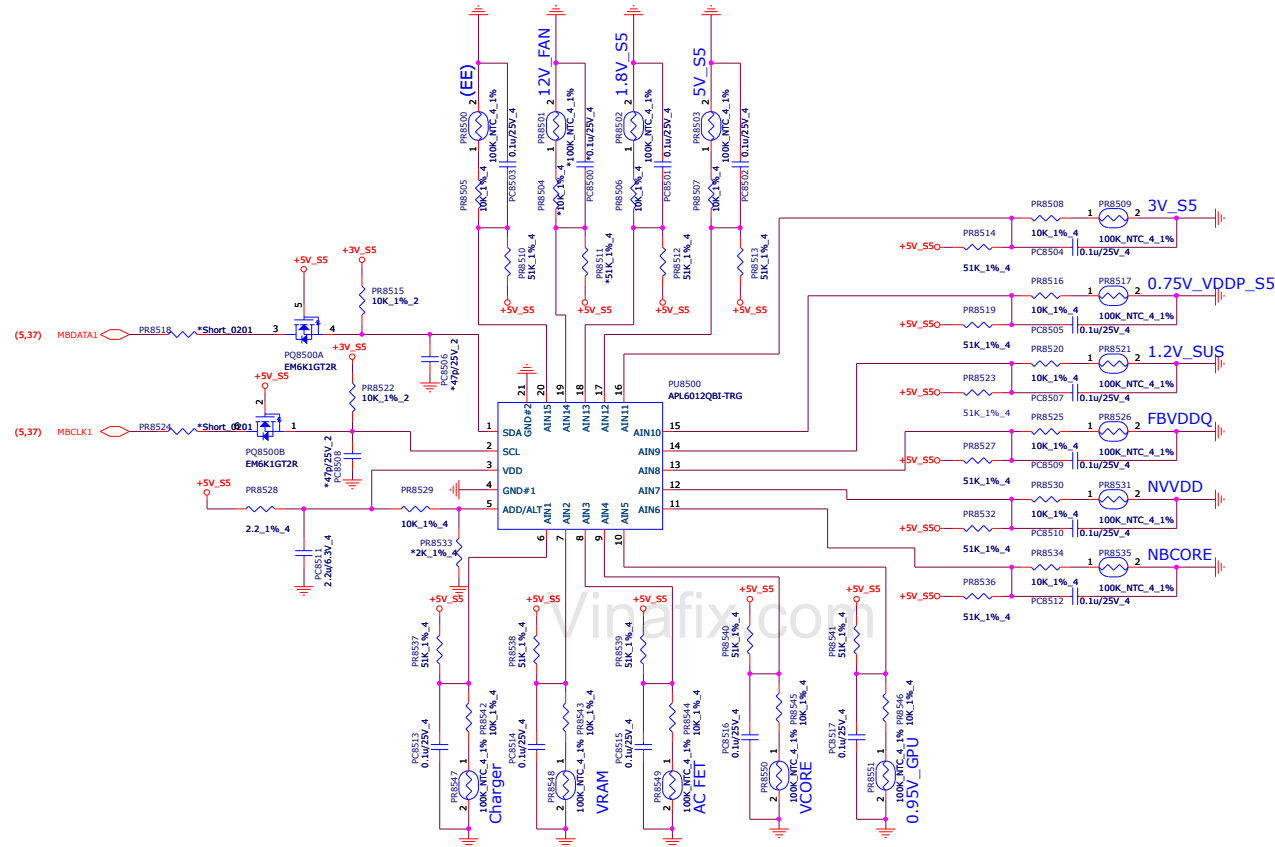
Vinafix.com

## Discharge

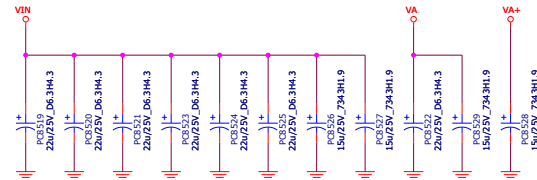


# OVR-M GEN2



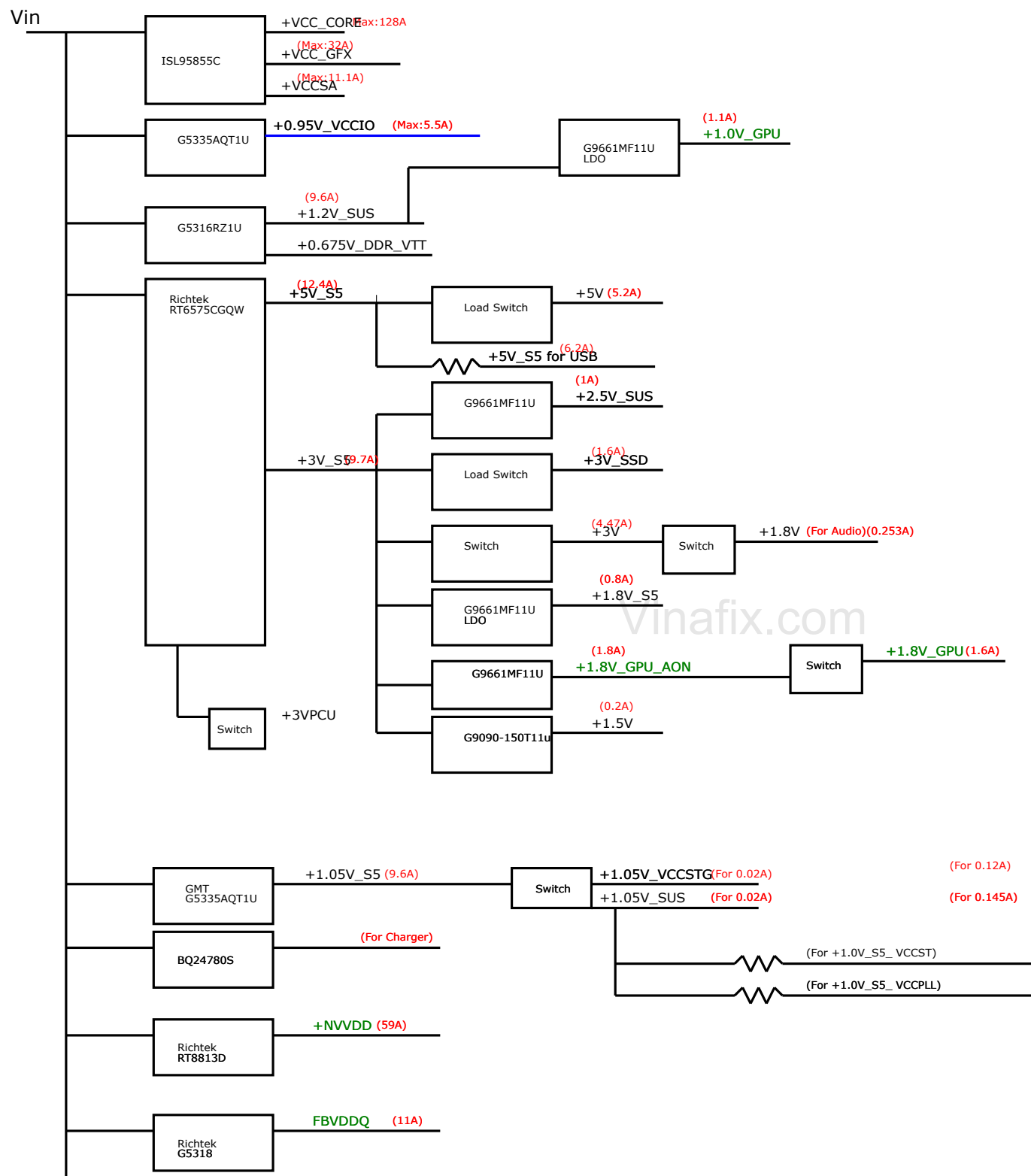


For ADP 200W

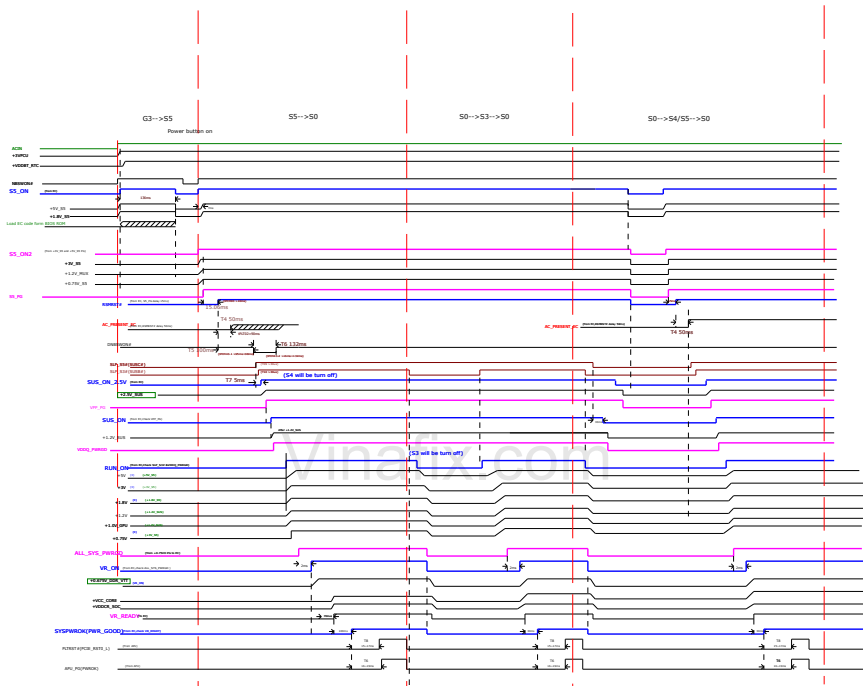


+12V for FAN Cancel

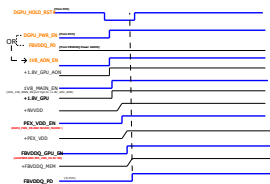
Vinafix.com







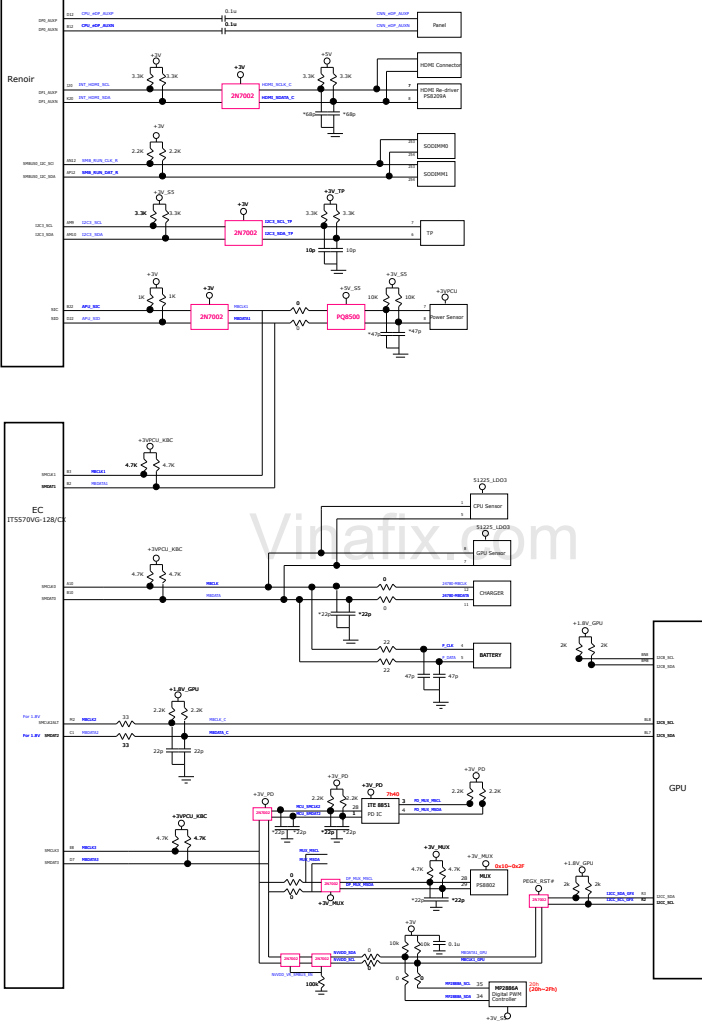
### N18P-G61/G62 Power-Up Sequencing



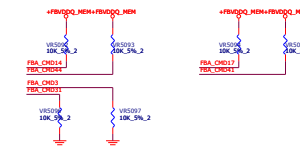
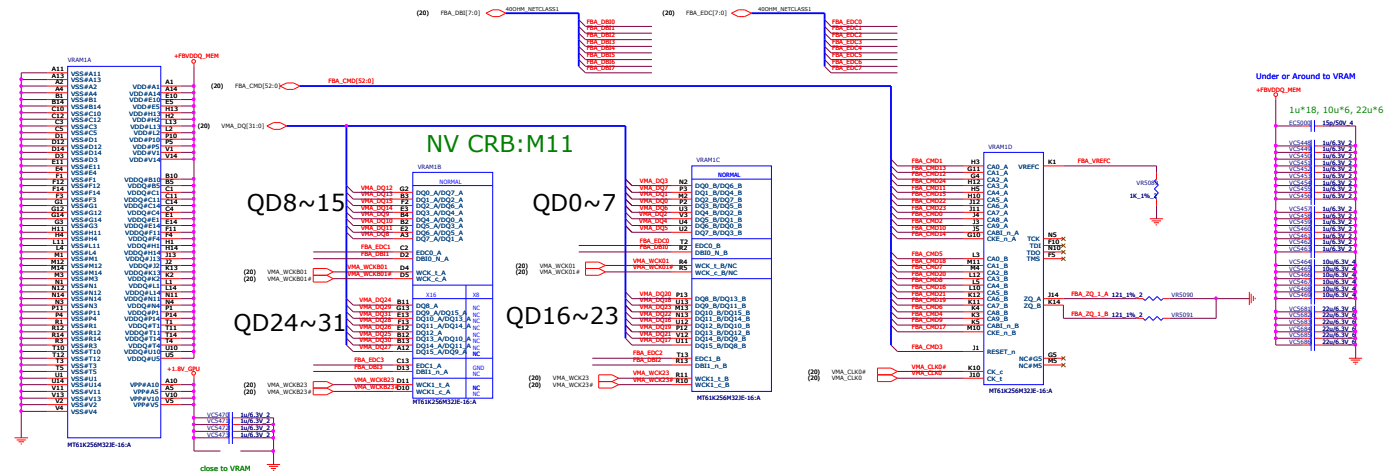
### N18P-G61/G62 Power-Down Sequencing (GC-OFF)



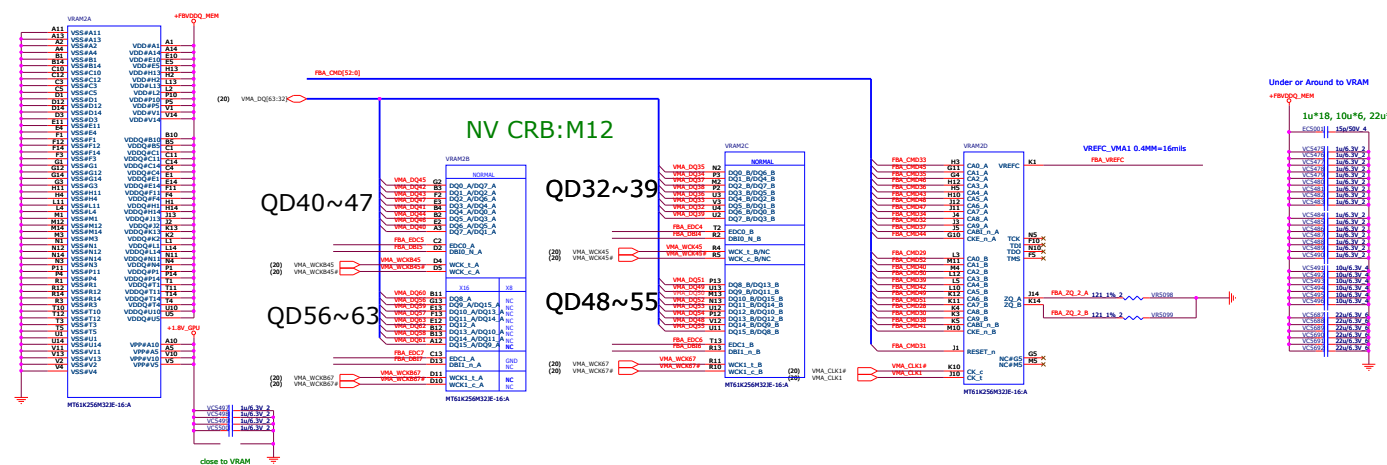
OS status	S0	S3		(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	S3		S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "y")	S5 (Fast Startup "x")	
RUN_ON	H	L		L	L	L	L	
+3V	H	L		L	L	L	L	
+5V	H	L		L	L	L	L	
+0.675V_DDR_VTT	H	L		L	L	L	L	
+12V	H	L		L	L	L	L	
+3V_SSD/+3V_PCH_CARD/+1.5V	H	L		L	L	L	L	
+1.05V_VCCSTG	H	L		L	L	L	L	
+VCCSA	H	L		L	L	L	L	
+VCC_GFX	H	L		L	L	L	L	
+VCC_CORE	H	L		L	L	L	L	
+0.95V_VCCIO	H	L		L	L	L	L	
SUS_ON	H	H		L	L	L	L	
+1.05V_VCCPLL/+1.05V_VCCST	H	H		L	L	L	L	
+1.05V_SUS	H	H		L	L	L	L	
+1.2V_SUS	H	H		L	L	L	L	
SUS_ON_2.5V	H	H		L	L	L	L	
+2.5V_SUS	H	H		L	L	L	L	
S5_ON	H	H		H	L	L	L	
+1.8V_S5	H	H		H	L	L	L	
+1.05V_S5	H	H		H	L	L	L	
S5_ON	H	H		H	L	H	L	
+3V_S5	H	H		H	L	H	L	
+5V_S5	H	H		H	L	H	L	



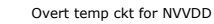




MEMORY: FBA Partition 63..32



GA1XX GDDR6 CMD Mapping		Upper 32.63 DRAM2 CHA-Byte 4,5
	Lower 0.31 DRAM1 CHA-Byte 0,1	
CAD_0	CM01	CM033
CAD_1	CM013	CM045
CAD_2	CM012	CM035
CAD_3	CM024	CM011
CAD_4	CM016	CM036
CAD_5	CM015	CM043
CAD_6	CM022	CM048
CAD_7	CM023	CM047
CAD_8	CM020	CM034
CAD_9	CM02	CM032
CAD_B	CM014	CM037
CAD_C	CM014	CM044
	CHB-Byte 2,3	CHB-Byte 6,7
CA0	CM08	CM029
CA1	CM018	CM052
CA2	CM07	CM040
CA3	CM020	CM050
CA4	CM01	CM039
CAS	CM016	CM042
CAS_B	CM08	CM049
CAS_7	CM09	CM051
CAS_8	CM06	CM028
CAS_B	CM04	CM030
CAB	CM019	CM038
CAB_B	CM017	CM041
CAB_C		
RESET*	CM03	CM031



Under GPU

Place Under VU1 for TOP side

VDD\_SENSE BT48  
VDD\_SENSE BT48

VGPU\_CORE\_SENSE  
VSS\_GPU\_SENSE

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